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Design of a Power-Efficient Routing-Based Approximate Multiplier Using Parallel Prefix Adder and Compressor

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ABSTRACT: Approximate computing has become an effective design methodology in order to develop high performance and energy-efficient digital signal processing (DSP) architectures as the issue of slight error in accuracy is no longer a concern. Of many components in DSP, the multiplier plays a significant role, as it has a direct contribution in regard to the power consumption, delay, and performance of the system. The paper proposes four energy-efficient Rounding-Based Approximate (RBA) multiplier architectures. The proposed architectures are able to approximate the input operands by rounding each to the closest power-of-two, such that the multiplication is performed using adding and shifting, instead of partial product generation and accumulation. Rounding the inputs leads to a less complex circuit overall, faster computing, and lower power dissipation. In addition to the four energy-efficient RBA multiplier architectures, one of the proposed architectures is a Reconfigurable Rounding-Based Approximate (RoBA) multiplier architecture that can increase the adaptability of both accuracy and energy efficiency, using a control signal. The proposed architectures were implemented and simulated in Verilog HDL utilizing Xilinx ISE 14.7 tools. Simulation results demonstrate that the proposed RBA and RoBA multipliers provide significant savings in power consumption and propagation delay in comparison to conventional multipliers, while still providing acceptable accuracy that is suitable for error-tolerant applications.

KEYWORDS: Digital Signal Processing (DSP), Rounding-Based Approximate (RBA) multiplier, rounding, adding and shifting, Verilog HDL, Xilinx ISE 14.7 tools, propagation delay.

I. INTRODUCTION

The growing demand for high energy-efficient digital signal processing (DSP) cores stems from the increasing use of multimedia applications in portable devices, primarily smartphones, which rely on small batteries. Multipliers are one of the more extensive components in DSP cores, meaning that their contribution to the overall power consumption and delay is significant. As a result, the pursuit of low-power, high-speed multipliers is a necessary solution for energy-efficient DSP systems. Approximately computing has become a viable design alternative for improved performance and lower power consumption with minimal impact on output quality, as many multimedia and image-processing applications are inherently error-tolerant. Approximation of arithmetic circuits can vary from the algorithmic level of an application to the architectural and circuit level. For this reason, approximate multipliers and adders have become a popular area of research to balance accuracy, performance, and power efficiency.

In the context of modern VLSI design, striking a balance between high throughput and low power consumption continues to be a significant issue. Conventional multipliers are precise, but require considerable power and area, which is not optimal for energy sensitive applications. The increasing need for improved operational performance for digital signal processing (DSP) in mobile, battery-powered, self-sustainable systems has necessitated alternative designs with better energy-performance trade-offs. Approximate computing, through various forms of rounding, presents a mechanism of simplification of complex arithmetic operations. This work presents an efficient RoBA multiplier design that reduces power and area, while maintaining acceptable levels of performance for a variety of applications, including image and video processing. This project intends to design and develop low-power, high-speed, area-efficient, Rounding-Based Approximate (RoBA) multiplier suitable for error-tolerant DSP applications. The focus here will be on evaluating a variety of RBA architectures for their delay, power, area, and energy efficiency against conventional



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multiplier architectures. The project aims to provide substantial enhancements in energy efficiency and speed of computation without severely impacting accuracy.

II. RELATED WORK

The Baugh–Wooley (BW) and Booth-encoded multipliers are among the most established architectures for signed binary multiplication. The radix-2 Baugh–Wooley multiplier provides a regular array structure that simplifies layout but suffers from high propagation delay due to a large number of partial products and a long carry-propagation chain.

To improve speed, the radix-4 Booth recoding (BR4) technique is adopted. Booth’s algorithm efficiently reduces the number of partial products by encoding consecutive bits of the multiplier. In the radix-4 version, two bits are processed at a time, effectively halving the number of partial products compared to the conventional radix-2 case. This significantly shortens the critical path and enhances computational throughput.

The radix-4 Booth recoding logic interprets the multiplier bits in overlapping triplets (x_{i+1}, x_i, x_{i-1}) and generates control signals to determine which multiples of the multiplicand should be added or subtracted in each stage. The operation table for Booth recoding is as follows:

Select Line	Operation
000	Add 0
001	Add multiplicand (x)
010	Add multiplicand (x)
011	Add 2×multiplicand (x)
100	Subtract 2×multiplicand (x)
101	Subtract multiplicand (x)
110	Subtract multiplicand (x)
111	Subtract 0

Table 2.1 Radix 4 booth recoding

This encoding reduces the total number of addition operations while maintaining the ability to handle signed numbers without explicit sign correction. The carry-save adder (CSA) tree or $(m,2)$ compressor structure is commonly used to accumulate partial products efficiently, followed by a carry-propagate adder (CPA) to produce the final product.

Although the Booth multiplier enhances speed and reduces area compared to the Baugh–Wooley architecture, it still consumes considerable power and introduces circuit complexity in the encoding and addition stages. Hence, it forms the baseline structure for further optimization in the proposed work.

The hardware implementation of the radix-4 Booth multiplier involves three main functional blocks:

- a) Booth Encoder and Decoder – Determines the operation (add/subtract/shift) based on the encoded multiplier bits.
- b) Partial Product Generator (PPG) – Generates multiplicand multiples as per the Booth encoding.
- c) Partial Product Reduction (PPR) – Combines the partial products using carry-save adders or compressor trees.

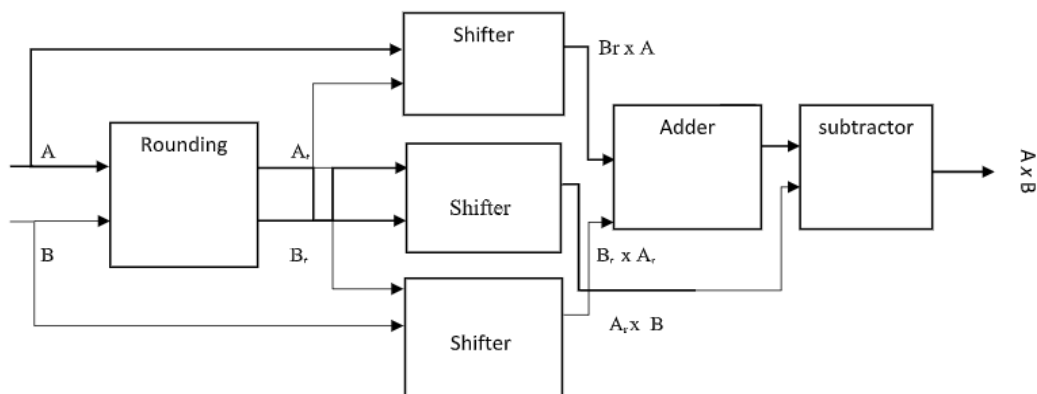


Figure 2.1 Block diagram for the hardware implementation of the existing multiplier



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A simplified block diagram of this structure (Figure 3.2) illustrates the data flow from input operands through the Booth encoder, PPG, and PPR to the final adder stage. Despite its improved efficiency, the design complexity scales rapidly with operand bit-width, leading to higher power consumption and longer delay for large-bit multiplications. To further improve performance, approximate computing principles are sometimes introduced in the rounding or truncation of operands before multiplication. In these designs, the operands are rounded to the nearest power-of-two (2^n), simplifying multiplication to a series of shift and add operations. This concept directly motivates the Rounding-Based Approximate (RBA) and Reconfigurable Rounding-Based Approximate (RoBA) multipliers developed in this work

III. PROPOSED WORK

The complexity of multiplication arises from the generation and accumulation of partial products. However, if the input operands are approximated to their nearest power-of-two equivalents, the multiplication operation can be realized using simple shift operations. This drastically simplifies the hardware architecture and minimizes energy consumption. Let the two input operands be represented as A and B, and their respective rounded power-of-two equivalents be A_r and B_r . The multiplication of A and B can be expressed as:

$$A \times B = A_r \cdot B + A \cdot B_r - A_r \cdot B_r + (A_r - A)(B_r - B) \quad \text{--- (1)}$$

Here:

- $A_r \cdot B$, $A \cdot B_r$, and $A_r \cdot B_r$ can be efficiently implemented using shift-and-add logic.
- The term $(A_r - A)(B_r - B)$ represents the rounding error, which contributes minimally to the final product when operands are efficiently rounded.
- By neglecting this small term, the multiplication can be approximated as:
- $A \times B \approx A_r \cdot B + A \cdot B_r - A_r \cdot B_r \quad \text{---(2)}$

This forms the basis of the Rounding-Based Approximation (RBA) approach.

PROPOSED ACCURACY-RECONFIGURABLE ROBA MULTIPLIER

To accommodate diverse application requirements, a Reconfigurable Rounding-Based Approximate (RoBA) multiplier is proposed. This architecture incorporates a control signal (CTL) that dynamically adjusts the trade-off between energy efficiency and computational accuracy.

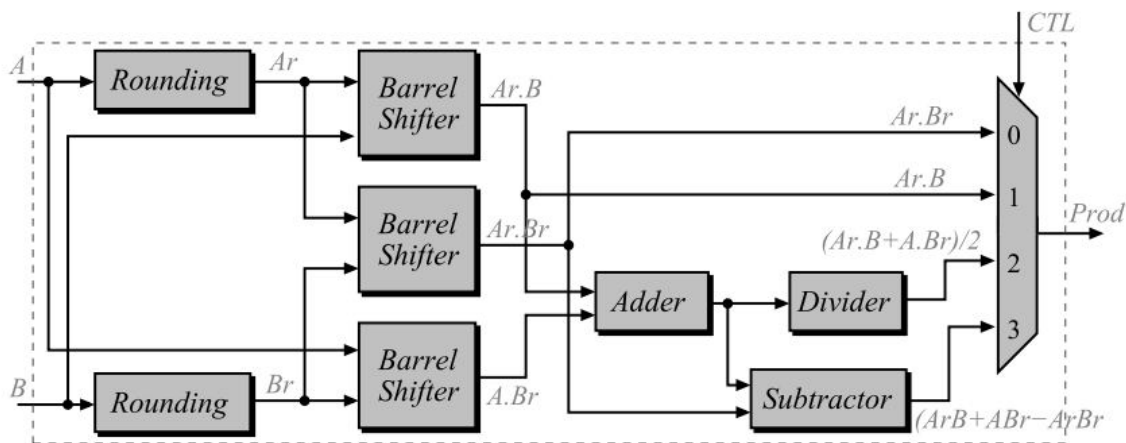


Figure 3.1 Proposed Reconfigurable RoBA

Depending on the CTL value, the architecture operates in one of four modes:



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Table 3.1 Operational Modes.

CCTL Value	Operation Mode	Equivalent Multiplier	Accuracy	Power Consumption
0	$Ar \times Br$	RBA0	Low	Very Low
1	$Ar \times B$	RBA1	Medium	Low
2	$(Ar \times B + A \times Br)/2$	RBA2	High	Moderate
3	$Ar \times B + A \times Br - Ar \times Br$	RBA3	Very High	Moderate-High

The reconfigurable feature allows the same hardware unit to adapt to different applications such as low-power image compression or high-precision DSP operations.

IV.SIMULATION RESULTS

In electronics, a hardware description language (HDL) is a specialized computer language used to program the structure, design and operation of electronic circuits, and most commonly, digital logic circuits. A hardware description language enables a precise, formal description of an electronic circuit that allows for the automated analysis, simulation, and simulated testing of an electronic circuit.

HDLs form an integral part of electronic design automation (EDA) systems, especially for complex circuits, such as microprocessors. HDLs are standard text-based expressions of the structure of electronic systems and their behaviour over time. Like concurrent programming languages, HDL syntax and semantics include explicit notations for expressing concurrency. However, in contrast to most software programming languages, HDLs also include an explicit notion of time, which is a primary attribute of hardware. Languages whose only characteristic is to express circuit connectivity between a hierarchy of blocks are properly classified as netlist languages used in electric computer-aided design (CAD). HDL can be used to express designs in structural, behavioral or register-transfer-level architectures for the same circuit functionality; in the latter two cases the synthesizer decides the architecture and logic gate layout.

HDLs are used to write executable specifications for hardware. A program designed to implement the underlying semantics of the language statements and simulate the progress of time provides the hardware designer with the ability to model a piece of hardware before it is created physically. It is this executability that gives HDLs the illusion of being programming languages, when they are more precisely classified as specification languages or modeling languages. Simulators capable of supporting discrete-event (digital) and continuous-time (analog) modeling exist, and HDLs targeted for each are available.



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VARIOUS SNAPSHOTS:

4.1 Device utilization summary: Area – Existing

MODELSIM TOOL

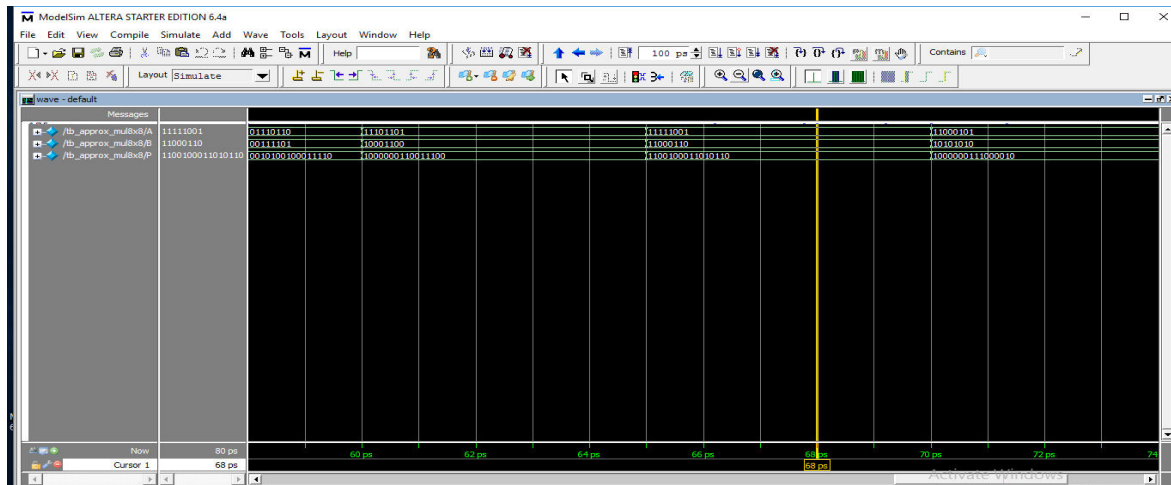


Figure 4.1 Design Summary of Existing 8 X 8 unsigned approximation Multiplier using modelsim

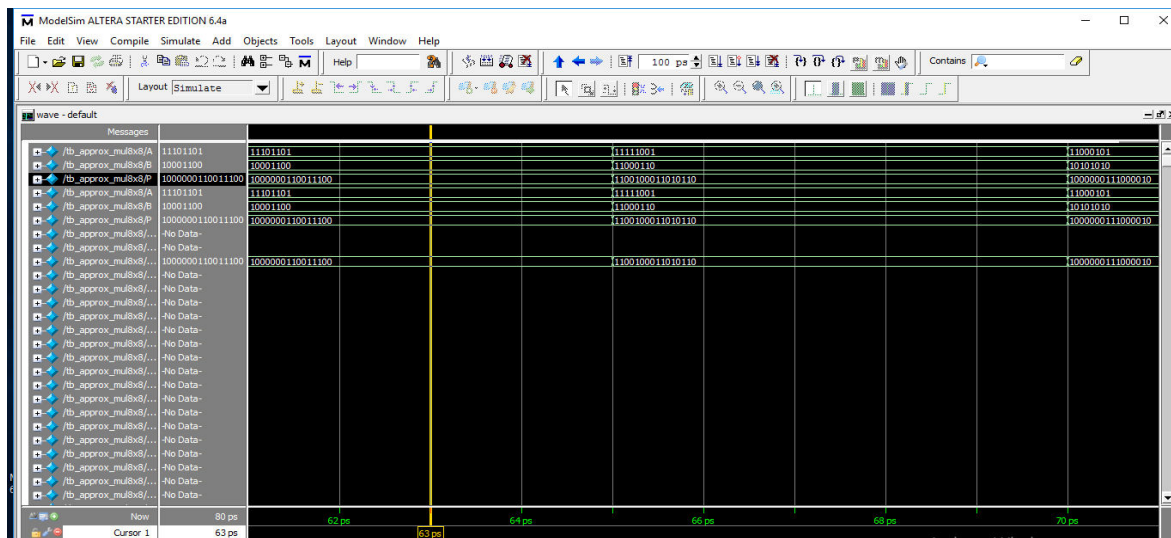


Figure 4.2 Simulation waveform proposed RoBA MULTIPLIER using MODEL SIM tool.

V.CONCLUSION AND FUTURE WORK

We proposed a high-speed yet energy efficient approximate multiplier called RoBA multiplier. The proposed multiplier, which had high accuracy, was based on rounding of the inputs in the form of 2^n . In this way, the computational intensive part of the multiplication was omitted improving speed and energy consumption at the price of a small error. The proposed approach is applicable to both signed and unsigned multiplications. The efficiencies of the proposed multipliers were evaluated by comparing them with those of approximate RoBA and accurate RoBA multipliers using different design parameters. The results revealed that, in most (all) cases, the RoBA multiplier architectures outperformed the corresponding approximate (exact) multipliers. The comparison revealed almost same image qualities as those of exact multiplication algorithms.



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VI. FUTURE WORK

In the future, novel design to advanced After performing the synthesise process, the RTL schematic has been created automatically based on the functionality. The routing between the different cells can be viewed clearly by this schematic. The proposed has been simulated and the synthesis report can be obtained by using Xilinx ISE 14.7.

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