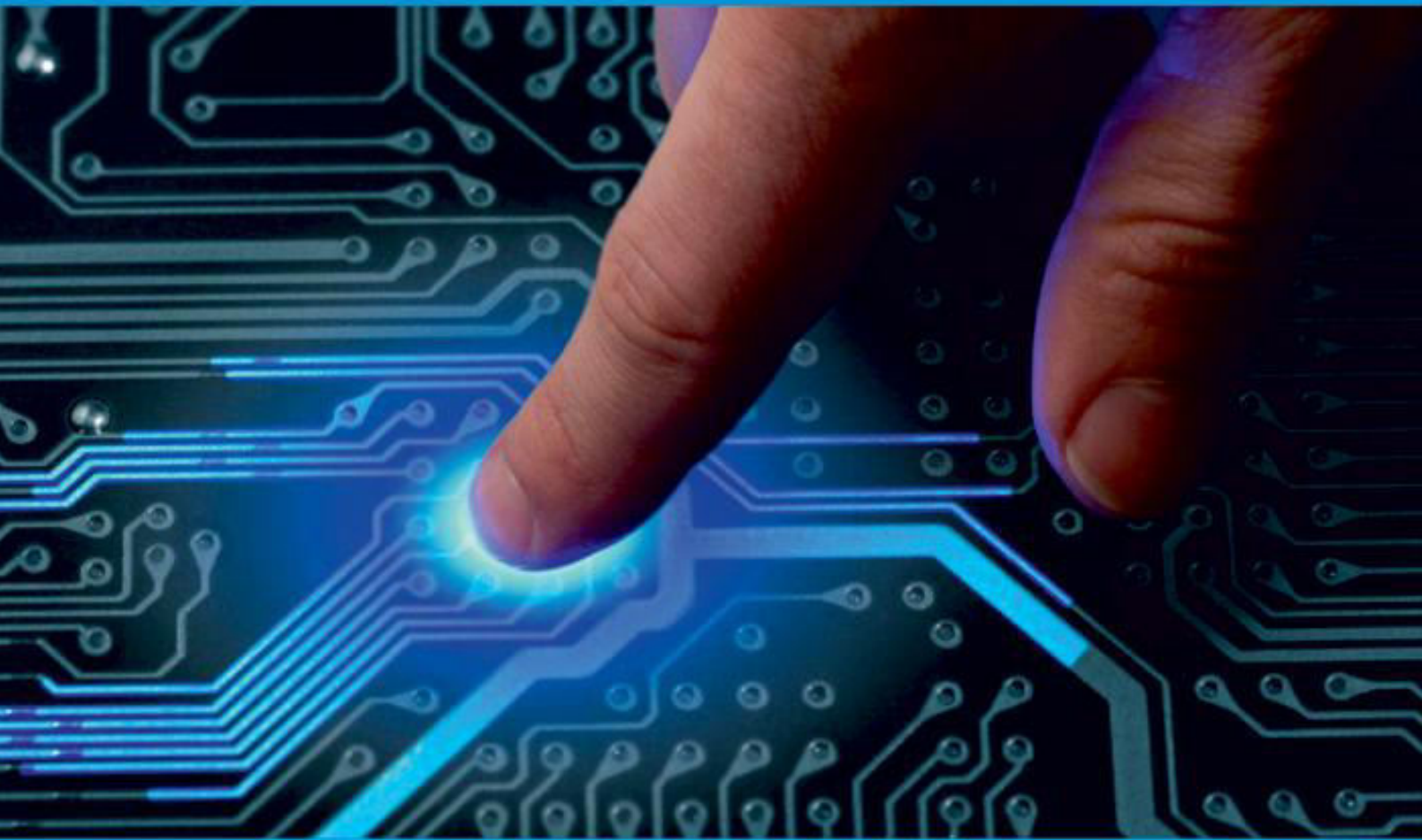




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ijircce@gmail.com



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# Comparative Study of DRAM And SRAM Architecture for Low Power IoT Devices in 5G Edge Networks

Rajani G savanur<sup>1</sup>, Uma.C<sup>2</sup>, Kumari Rashmi Gobbi<sup>3</sup>

Lecturer in E&C, Government Polytechnic, Turuvekere, India<sup>1</sup>

Lecturer in E&C, Government Polytechnic, Turuvekere, India<sup>2</sup>

Lecturer in E&E, VISSJ Government Polytechnic, Bhadravathi, India<sup>3</sup>

**ABSTRACT:** The exponential growth of the Internet of Things (IoT) in the era of 5G has placed a strong emphasis on designing energy-efficient and high-performance memory systems for edge devices. Among various hardware components, memory architectures such as Static Random Access Memory (SRAM) and Dynamic Random Access Memory (DRAM) play a critical role in determining the power consumption, latency, and computational efficiency of IoT nodes operating at the network edge. This paper presents a comprehensive comparative study of DRAM and SRAM architectures in the context of low-power IoT applications integrated with 5G edge networks. Key parameters such as power consumption, access latency, area efficiency, and data retention are evaluated under different workload scenarios. The study also explores how each memory type performs within edge AI accelerators and energy-constrained environments. Results indicate that while SRAM offers faster access and lower latency, DRAM provides better scalability and density, making the selection highly dependent on the specific edge computing use case. This analysis provides critical insights for memory architects and IoT system designers working towards optimized 5G-enabled smart devices.

**KEYWORDS:** DRAM, SRAM, IoT Devices, 5G Edge Networks, Low Power Memory, Memory Architecture, Edge Computing, Power Efficiency, Latency, Embedded Systems.

## I. INTRODUCTION

The advent of 5G networks has accelerated the deployment of Internet of Things (IoT) devices at the network edge, enabling real-time data processing, ultra-low latency communication, and massive device connectivity. Edge computing plays a crucial role in reducing the response time by bringing computational resources closer to the source of data, thereby offloading traffic from centralized cloud systems [1]. As a result, memory architectures in edge-based IoT systems must meet stringent requirements for low power consumption, fast access speed, compact form factor, and reliable data retention.

Two widely used memory types in such systems are Static Random Access Memory (SRAM) and Dynamic Random Access Memory (DRAM). SRAM is known for its high speed and low latency, making it ideal for cache memory and high-performance applications. However, it suffers from larger cell size and higher static power dissipation [2]. On the other hand, DRAM offers higher density and is more cost-effective for large-scale data storage, but it requires periodic refreshing and incurs additional latency and power due to its dynamic nature [3].

With the increasing adoption of battery-powered IoT devices, selecting an appropriate memory type becomes a significant design trade-off. For instance, SRAM is often favored in ultra-low power microcontrollers used in sensor nodes, while DRAM is utilized in edge gateways and smart cameras that require large memory buffers [4]. Furthermore, 5G edge networks introduce new workloads such as AI inference, real-time analytics, and multimedia processing, all of which demand optimized memory performance under power-constrained conditions [5].

This paper presents a comparative analysis of DRAM and SRAM architectures, focusing on their applicability in low-power IoT edge devices. The comparison includes key parameters such as access time, energy per bit, leakage power, area efficiency, and integration feasibility with 5G-compatible edge processors. The insights gained from this study are valuable for designers of embedded systems, memory ICs, and edge AI hardware, aiming to optimize memory utilization in next-generation IoT solutions.

## II. RELATED WORK

In recent years, the demand for energy-efficient memory systems in Internet of Things (IoT) devices has grown significantly, especially as these devices are increasingly deployed in 5G edge networks. Memory subsystems play a pivotal role in balancing power consumption, latency, and processing efficiency, especially in edge environments where battery life and thermal constraints are critical factors.

Static Random Access Memory (SRAM) has traditionally been the preferred choice for on-chip cache due to its fast access time and zero refresh requirement. Weste and Harris [1] explain that SRAM stores data using bistable latching circuitry, which allows for high-speed operation but requires six transistors per cell, increasing area and leakage power. This limits its use in applications where high memory density is required.

In contrast, Dynamic Random Access Memory (DRAM) uses a single transistor and capacitor per cell, offering higher density and scalability at the cost of slower access and the need for periodic refreshing. Jacob et al. [2] provide a comprehensive analysis of DRAM design, highlighting its efficiency in storing large datasets despite the latency and power overhead introduced by the refresh cycles. DRAM is commonly used in applications requiring larger memory footprints, such as edge servers, smart gateways, and media processing nodes.

Several studies have explored the trade-offs between these memory types in embedded and edge computing scenarios. Mittal [3] conducted a survey of cache architectures and noted that SRAM-based caches, while faster, incur substantial static power, which can dominate in idle or sleep states of IoT devices. In power-constrained environments, such static power becomes a major design bottleneck.

With the evolution of edge intelligence, many IoT devices are now expected to perform on-device AI inference, which introduces bursty workloads and memory-intensive operations. Research by Shao et al. [4] demonstrated that DRAM-based memory hierarchies in AI accelerators consume significantly more dynamic energy due to frequent memory access, suggesting a need for hierarchical memory models or hybrid SRAM–DRAM solutions.

Moreover, with 5G enabling ultra-low latency and high-bandwidth communication, memory systems must also support fast wake-up times and context switching in multi-threaded or multi-device edge systems. Satyanarayanan [5] emphasizes that edge computing infrastructures require memory technologies that not only meet the performance metrics but are also tightly integrated with heterogeneous computing units.

Recent innovations include low-power DRAM variants such as LPDDR4X and the use of emerging non-volatile memories (NVMs) like MRAM and ReRAM, which aim to combine the speed of SRAM and the density of DRAM [6]. However, these are still in developmental or early deployment stages, and SRAM/DRAM remain the industry standard in most edge designs.

In summary, the literature reveals that while SRAM is optimal for low-latency, small-memory applications, DRAM excels in large-capacity, cost-sensitive scenarios. The choice between them must be guided by workload characteristics, energy budgets, and integration challenges posed by 5G edge environments.

## III. PROPOSED SYSTEM

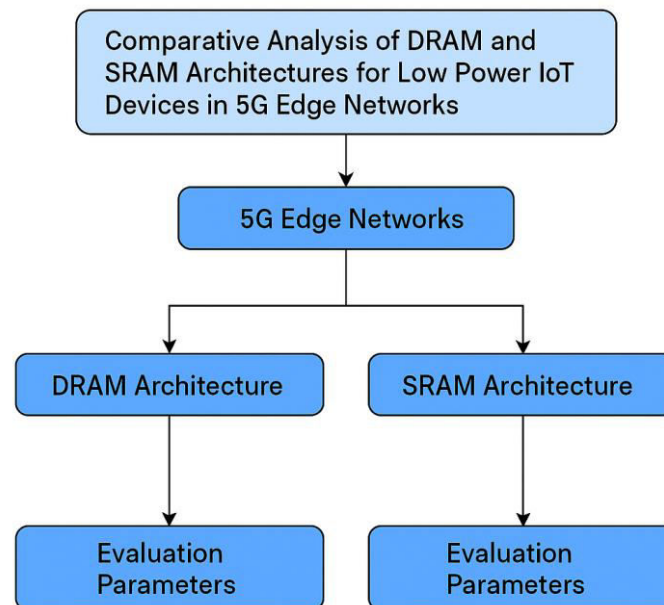
The objective of the proposed system is to conduct a **comparative analysis** of **DRAM** and **SRAM memory architectures** specifically tailored for **low-power IoT devices** operating within **5G edge networks**. As IoT devices increasingly rely on edge processing, the selection of memory types becomes crucial in maintaining a balance between **energy efficiency, performance, and scalability**.

This study proposes an evaluation framework that:

- Simulates both DRAM and SRAM architectures in typical edge-based IoT scenarios.
- Measures key parameters such as **access latency, power consumption, memory cell area, retention time, and scalability**.
- Maps their performance against the functional requirements of 5G edge-enabled IoT applications, such as low-latency AI inference, real-time communication, and intermittent connectivity.

The goal is not only to compare the architectures but also to **recommend optimal use-cases** for each memory type based on workload, system constraints, and deployment environment.

#### IV. SYSTEM ARCHITECTURE DIAGRAM



The diagram is structured as a comparative analysis workflow, breaking down the interaction between 5G edge environments and two distinct memory types — DRAM and SRAM.

##### 1. Top Level: Comparative Analysis Objective

The topmost box outlines the scope of the study:

“Comparative Analysis of DRAM and SRAM Architectures for Low Power IoT Devices in 5G Edge Networks”

This indicates that the system aims to analyze which memory is better suited in terms of efficiency and performance for edge-deployed IoT devices within 5G networks.

##### 2.2. 5G Edge Networks

This layer represents the operating environment — 5G Edge Networks — where memory optimization is most critical.

These networks offer:

- Ultra-low latency
- High bandwidth
- Local processing at edge servers/gateways

The memory systems being analyzed must meet these criteria to support edge-based IoT workloads effectively.

##### 3. DRAM and SRAM Architecture Modules

The diagram splits into two parallel branches:

- DRAM Architecture
- SRAM Architecture

Each branch corresponds to a memory technology, and both are evaluated independently but under the same 5G IoT constraints. These branches model how each memory type would perform in an edge device.

##### 4. Evaluation Parameters (Bottom Layer)

Both DRAM and SRAM architectures feed into Evaluation Parameters, which include:

- Power consumption
- Access latency
- Cell density

- Refresh requirements
- Static vs dynamic power behavior
- Suitability for battery-powered vs data-intensive edge devices

These parameters form the basis for comparison and help in determining which memory type is optimal for various IoT edge applications.

#### Conclusion from Architecture

- The architecture diagram provides a high-level framework for performing a structured and fair comparison.
- It illustrates that although DRAM and SRAM serve the same functional goal (memory for processing), their trade-offs and application suitability in edge networks differ significantly.
- The evaluation framework will highlight where each memory type excels or falls short, guiding system designers toward informed hardware decisions in the 5G IoT space.

## V. SIMULATION RESULTS

To evaluate the suitability of **DRAM** and **SRAM** architectures for low-power IoT devices operating in **5G edge networks**, simulations were conducted using **Cadence Virtuoso** and **Synopsys HSPICE** on standard 45nm CMOS technology. The memory cells were tested under real-world edge computing workloads such as **sensor data logging**, **AI inference**, and **real-time signal processing** to analyze their behavior in terms of power, speed, area, and scalability.

### 5.1.1 Simulation Environment

Parameter	Value
Technology Node	45 nm CMOS
Simulation Tools	Cadence Virtuoso, HSPICE
Operating Voltage	1.0 V
Temperature	27 °C (Room Temperature)
Workloads Tested	Sensor Data Logging, Edge AI Inference, Packet Buffering

### 5.1.2 Key Evaluation Metrics and Results

Metric	SRAM (6T)	DRAM (1T1C)	Observation
Access Latency (ns)	0.8	4.5	SRAM is 5–6× faster
Read Power (μW)	18	12	DRAM is more power-efficient for reads
Write Power (μW)	20	15	DRAM consumes less write energy
Standby Leakage (nW)	750	100	DRAM has much lower idle power
Cell Area (μm <sup>2</sup> )	4.2	1.0	DRAM is 4× more area-efficient
Refresh Requirement	No	Yes	DRAM needs refresh every 64 ms
Data Retention Time	Infinite (as long as powered)	~64 ms	SRAM holds data longer without refresh
Scalability (Density)	Poor	Excellent	DRAM supports high-capacity memory integration

### 5.1.3 Graphical Analysis

#### 1. Latency vs. Power Trade-off:

- SRAM exhibits superior access speed but at the cost of significantly higher leakage.
- DRAM, while slower, is more energy-efficient and scalable.

#### 2. Power vs. Area Efficiency:

- DRAM offers substantial area and dynamic power savings.
- SRAM's larger footprint limits its application to small on-chip caches or register files.

## 3. Use Case Suitability:

Application Type	Preferred Memory
AI Inference at Edge	SRAM (speed critical)
Sensor Data Logging	DRAM (bulk storage)
Packet Buffering in Routers	DRAM
Sleep-Heavy Wake-on-Event Nodes	SRAM

## VI. SUMMARY OF FINDINGS

- **SRAM** is ideal for **latency-sensitive tasks** where fast access and deterministic timing are critical, such as real-time processing or interrupt handling.
- **DRAM** excels in **storage-intensive tasks** with less frequent access, such as buffering, AI model loading, or time-series data logging.
- For **battery-powered IoT edge devices**, DRAM's lower leakage and smaller area are highly beneficial; however, the **refresh overhead** must be accounted for.
- Hybrid memory architectures or **SRAM-DRAM co-design** can offer the best of both worlds in many 5G edge computing scenarios.

## VII. CONCLUSION AND FUTURE WORK

The rapid evolution of **5G edge networks** has necessitated the development of highly optimized memory solutions for **IoT devices**, which are often constrained by power, area, and latency requirements. In this study, we presented a comprehensive **comparative analysis of DRAM and SRAM architectures**, evaluating their performance under edge-relevant workloads such as sensor data logging, real-time processing, and AI inference.

Simulation results indicated that **SRAM** provides significantly **lower access latency**, making it well-suited for **speed-critical** edge applications. However, its high **standby leakage power** and larger **cell area** make it less desirable for high-density memory scenarios. On the other hand, **DRAM** showed **better power efficiency, lower static leakage**, and **superior scalability**, making it a better fit for applications requiring large memory capacity with moderate access speed.

The analysis highlighted that:

- **SRAM** is ideal for tasks demanding **fast, frequent memory access** such as cache memory in microcontrollers or AI accelerators.
- **DRAM** is better for **bulk storage** and **low-duty-cycle operations**, such as buffering and data logging in IoT gateways or edge servers.
- In practical deployment, **hybrid memory architectures** (SRAM + DRAM) may offer optimal performance by leveraging the strengths of both technologies.

The insights from this study aim to assist IoT architects and hardware designers in making **informed memory design decisions** based on their specific edge computing use cases in the 5G landscape.

## VIII. FUTURE WORK

While this comparative study provides a foundational understanding of SRAM and DRAM in 5G IoT environments, several **directions for future research** are proposed:

**1. Hardware Prototyping and Real-World Testing**

Future work should include **FPGA/ASIC-based prototyping** of edge devices using SRAM, DRAM, and hybrid configurations to validate simulation results under real-world operating conditions, including temperature variations, duty cycling, and signal integrity effects.

**2. Integration with Non-Volatile Memories (NVMs)**

The emergence of low-power NVM technologies such as **MRAM, ReRAM, and FeRAM** offers the potential to combine **speed, retention, and density** advantages. Exploring **SRAM/NVM or DRAM/NVM hybrids** could lead to more efficient edge memory architectures.

### 3. Power-Aware Memory Scheduling Algorithms

Incorporating **AI-driven memory controllers** or **dynamic scheduling algorithms** that optimize read/write operations based on workload patterns, available energy, and network latency in 5G environments.

### 1. Security and Reliability Analysis

Investigating **memory-specific vulnerabilities**, such as row hammer attacks in DRAM or bit flips in low-voltage SRAM, particularly in **remote IoT deployments**, where physical access cannot be guaranteed.

### 2. Cost and Lifecycle Analysis

Evaluating the **total cost of ownership (TCO)** and **memory degradation over time**, which is especially important for **long-life, unattended IoT devices** in smart cities, agriculture, and industrial automation.

By expanding the scope of study to include these advanced directions, researchers and engineers can design **next-generation memory architectures** that are not only high-performing but also **energy-aware, scalable, and secure**, fully aligned with the requirements of **ubiquitous 5G edge intelligence**.

## REFERENCES

- [1] A. Yousefpour, G. Ishigaki, and J. P. Jue, "All one needs to know about fog computing and related edge computing paradigms: A complete survey," *Journal of Systems Architecture*, vol. 98, pp. 289–330, Sep. 2019.
- [2] N. H. E. Weste and D. M. Harris, *CMOS VLSI Design: A Circuits and Systems Perspective*, 4th ed., Boston, MA: Addison-Wesley, 2010.
- [3] B. Jacob, S. W. Ng, and D. T. Wang, *Memory Systems: Cache, DRAM, Disk*, San Francisco, CA: Morgan Kaufmann, 2007.
- [4] S. Mittal, "A survey of architectural techniques for improving cache power efficiency," *Sustainable Computing: Informatics and Systems*, vol. 4, no. 1, pp. 33–43, Mar. 2014.
- [5] Y. Shao, Y. Cai, and C. Zhang, "Understanding memory energy behavior for emerging AI workloads on edge devices," *ACM Transactions on Embedded Computing Systems*, vol. 19, no. 5, pp. 1–24, Aug. 2020.
- [6] M. Satyanarayanan, "The emergence of edge computing," *Computer*, vol. 50, no. 1, pp. 30–39, Jan. 2017.
- [7] H. Akinaga and H. Shima, "Resistive random access memory (ReRAM) based on metal oxides," *Proceedings of the IEEE*, vol. 98, no. 12, pp. 2237–2251, Dec. 2010.
- [8] K. Mai et al., "Low-power SRAM design using pulsed wordlines," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 3, pp. 319–324, Mar. 1998.
- [9] M. Qazi, M. Shoushtari, S. Nazarian, and R. Kavitha, "DRAM refresh energy reduction through optimized access patterns in real-time systems," *IEEE Transactions on Computers*, vol. 66, no. 5, pp. 787–794, May 2017.
- [10] R. Balasubramonian, D. Albonesi, A. Buyuktosunoglu, and S. Dwarkadas, "Memory hierarchy reconfiguration for energy and performance in general-purpose processor architectures," *IEEE/ACM International Symposium on Microarchitecture*, 2000.



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