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Design of 64 Bit Low Power Reversible Comparator

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ABSTRACT: In recent years, low power, less area and high speed are prime focuses for digital VLSI Circuits and in DSP applications. Comparator is very important block in analog to digital converters, null detectors, zero crossing detectors, level shifter, window detectors, ALU, and microprocessor/controller. Reversible logic has received attention in the recent years due to their ability to reduce the power dissipation which is the main requirement in low power VLSI design. The promising esteems of reversible circuitry corroborates the notion of loss less information processing, low power consumption, high speed computing and least garbage value generation.A comparator is a device used to compare two numbers and produce the result. The comparator is designed by using the combinational logic gates. The limitation of this approach is that it results in huge transistor count which increases the area of circuit. The usage of Gate Diffusion Input (GDI) cells reduces the area of circuit.

KEYWORDS: GDI, Digital Comparator

I. INTRODUCTION

As the trend for low power has begun in the world of electronics, power dissipation along with performance is one of the design constraints in nanometer technologies. The development in VLSI technology facilitated developing a portable device due to incorporation of a complete system on chip. In battery operated portable device, power dissipation is one of the critical parameters. The limited battery life time imposed demands on the overall power consumption of the portable systems. The power dissipation of a chip depends on the technology, its implementation, operating frequency, circuit style, and size etc… Increase in the usage of battery operated devices like mobiles and laptops creates a need to reduce size and power dissipation along with the device performance. Comparators play a vital role in DSP applications. Digital comparators or binary comparators are designed by using standard AND, XOR, NOT gates.

Section II gives information about comparator. Section III describes the reversible logic. Results and comparison of technologies are discussed in section IV. Section V and section VI consists of conclusion and references respectively.

II. COMPARATOR

In computer systems and device interfaces, comparing two binary words is the commonly used operation. A circuit that compares two words and indicates equality between them is known as comparator. Magnitude comparators are the comparators that indicate arithmetic relationship (greater or less than) between the words. Exclusive – OR and Exclusive – NOR gates can be observed as 1-bit comparators.To perform comparison of two operands A and B of longer lengths, more than 1 comparator can be connected in cascade arrangement. While comparing two binary numbers, the more significant bits must be compared in prior. If these MSB's are equal , then the next bits will be compared but if the MSB's are not equal, then it would be clear that either A is greater or less than B. For example, consider A=A1A0, B=B1B0, if A1 is not equal to B1, then it is evident that A>B for A1=1 and B1=0 else A<B. If MSB's are equal, then the next significant bits are compared. If A1=B1, then A0 and B0 are compared and three outputs greater than, less than and equal to are produced.

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In this design approach, the comparator consists of series of reversible cells to compare a single bit. To construct a 64 bit comparator we use BJS gate, HLN and LT gates. The 64 bit comparator is formed by integration of GE cells, BJS cell and LT cell.

a) *HLN gate*:

HLN gate is a 3 X 3 gate. The gate is shown in the fig 1 and corresponding truth table in table 1.

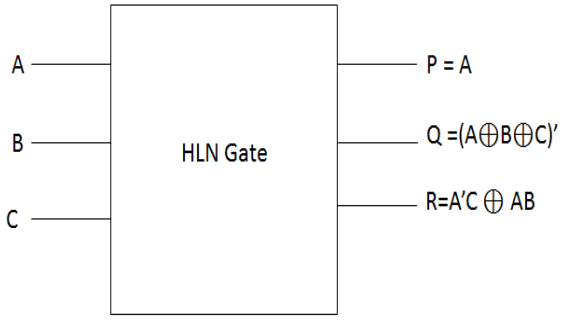

Figure 1 : HLN gate

When input bit C=1 it performs EXOR (Q=) and when C=0 it performs AND (R=AB) operations. HLN gate along with Peres(PG) gate is used in the construction of GE cell.

Table 1 : Truth table of HLN gate

A	B	C	P	Q	R
0	0	0	0	1	0
0	0	1	0	0	1
0	1	0	0	0	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	1	0	1

b) BJS gate: A 4 X 4 reversible gate namely BJS gate is used for most significant bit comparison. The gate is shown in the fig 2 and the corresponding truth table in table 2.

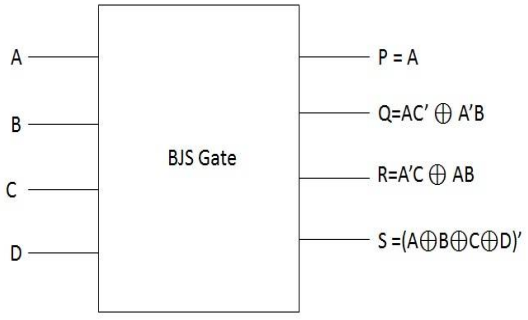

Figure 2: Block diagram of BJS gate

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When B=0 and D=0, Q= A′B; R= AB′; S= (A⊕B)'. When the bits B and D are logical zero, the BJS gate acts as a comparator with output bit Q implying greater than, R less than and S bit implying equal to operation.
When B=0 and D=0, BJS gate acts as a one bit comparator. Figure 3 shows the 1-bit comparator and the truth table is shown in table 3.

Table 2 : Truth table of BJS gate

A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	1
0	0	0	1	0	0	0	0
0	0	1	0	0	0	1	0
0	0	1	1	0	0	1	1
0	1	0	0	0	1	0	0
0	1	0	1	0	1	0	1
0	1	1	0	0	1	1	1
0	1	1	1	0	1	1	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	0	0	1
1	0	1	1	1	0	0	0
1	1	0	0	1	1	1	1
1	1	0	1	1	1	1	0
1	1	1	0	1	0	1	0
1	1	1	1	1	0	1	1

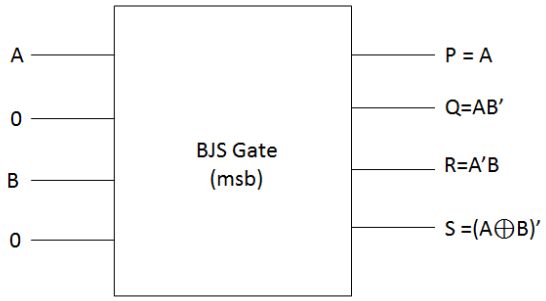

Figure 3: Block diagram of 1-bit comparator

Table 3: Truth table of 1-bit comparator

A	B	AGB	AEB	ALB
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0

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c) GE cell

The fig 3 shows a greater than equal to(GE) comparator cell. This cell is constructed using a HLN cell and two PG gates as shown. Depending upon the previous inputs, this cell compares the (n-1)bit of the input and produces two outputs pn-1(AGB) and qn-1(A=B) indicating greater than or equal to each other. The truth table of GE cell is shown in the table 4.

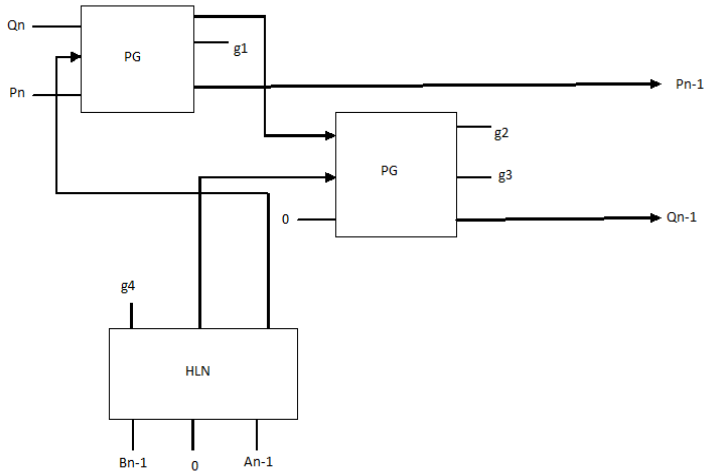

Figure 4: Block diagram of GE cell.

Table 4: Truth table of GE cell.

P_n	Q_n	B	A	P_{n-1}	Q_{n-1}
0	0	0	0	0	0
0	0	0	1	0	0
0	0	1	0	0	0
0	0	1	1	0	0
0	1	0	0	1	0
0	1	0	1	1	0
0	1	1	0	1	0
0	1	1	1	1	0
1	0	0	0	0	1
1	0	0	1	1	0
1	0	1	0	0	0
1	0	1	1	0	1
1	1	0	0	1	1
1	1	0	1	0	0
1	1	1	0	1	0
1	1	1	1	1	1

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d) LT cell

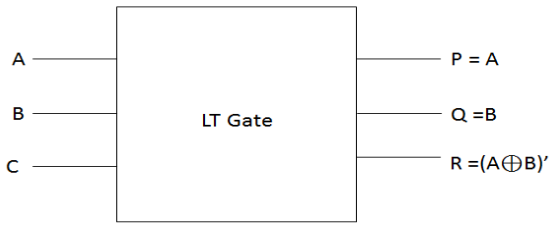

Figure 5 : Block diagram of LT gate

The fig 5 shows an single bit LT (Less than) cell. If a number is less than the other, it is neither equal nor greater than. Hence, ALB = (AGB⊕AEB)′. The outputs pn and qn from the previous cell acts as inputs and produces the outputs greater than, equal to and less than. The truth table of this 3 X 3 cell is shown in the table 5.

Table 5: Truth table of LT gate

A	B	P	Q	R
0	0	0	0	1
0	1	0	1	0
1	0	1	0	0
1	1	1	1	1

e) 2- bit comparator:

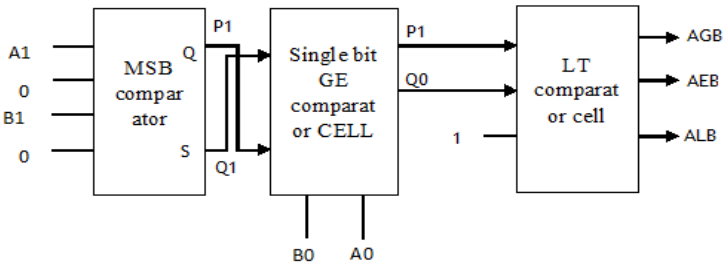

Figure 6: Block diagram of 2-bit comparator

f) 64- bit comparator:

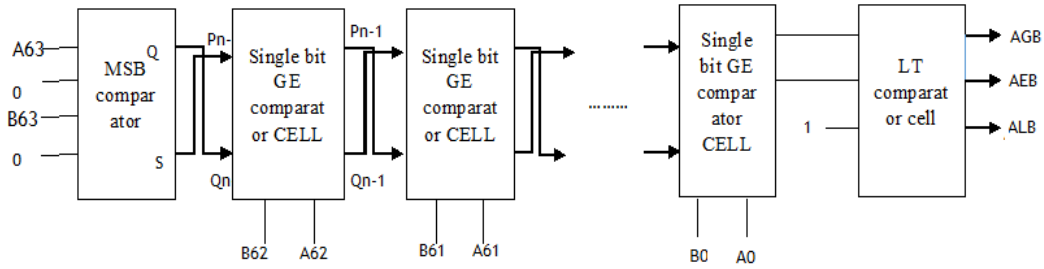

Figure 7 : Block diagram of 64 bit comparator

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Figure 7 shows the block diagram of 64 bit comparator. The 64 bit comparator is a combination of BJS gate, 63 GE cells and a LT cell. The inputs from the BJS gate are provided subsequently to the GE cells. The output from the last GE cell is provided to the LT cell.

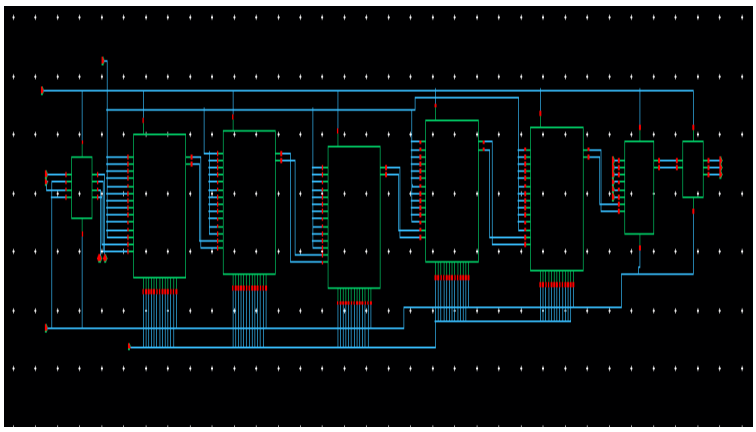

Figure 8: Block diagram of 64 bit comparator implemented in Cadence tool.

III. REVERSIBLE LOGIC

Energy loss is an important consideration in digital circuit design, higher levels of integration and the use of new fabrication processes have dramatically reduced the heat loss over the last decades. The other part of the problem arises from Landauer's principle for which there is no solution. According to Landauer's principle, the logic computations that are not reversible necessarily generate kT* ln 2 Joules of heat energy for every bit of information that is lost, where k is Boltzmann's constant and T the absolute temperature at which computation is performed. For room temperature T the amount of dissipating heat is small at (i.e. 2.9 $*10^{-21}$ Joules). This amount of heat loss may seem to be insignificant, but will become relevant in the future. According to second law of thermodynamics, Heat dissipated by the physically reversible circuit is zero. Theoretically, a reversible circuit is a circuit with no heat dissipationA reversible logic circuit should have the following features:

Definition 1: An n input, m output logic gate, is said to be reversible if there is a one-to-one correspondence between its inputs and outputs.

Definition 2: A gate is reversible if it maps each input vector into a unique output vector and vice versa i.e., the function is bijective.

Definition 3: An additional output, that are not used or unwanted, that makes an n-input m-output function reversible is called garbage bit (G).

Definition 4: Ancilla are the number of ancillary inputs, which are constant inputs and are used to maintain the reversibility of the circuit.

Definition 5: Quantum cost (QC) of a gate is the number of elementary quantum operations that are used to implement the complete functionality. All elementary 1 x 1 and 2 x 2 qubit gates have quantum cost of 1

IV. RESULTS AND COMPARISON

The 64 bit comparator is simulated using cadence virtuoso tool. The design is implemented using gdpk 45nm technology and gdpk 180nm technology. The simulation output of the 64 bit comparator is shown in the figure 9.

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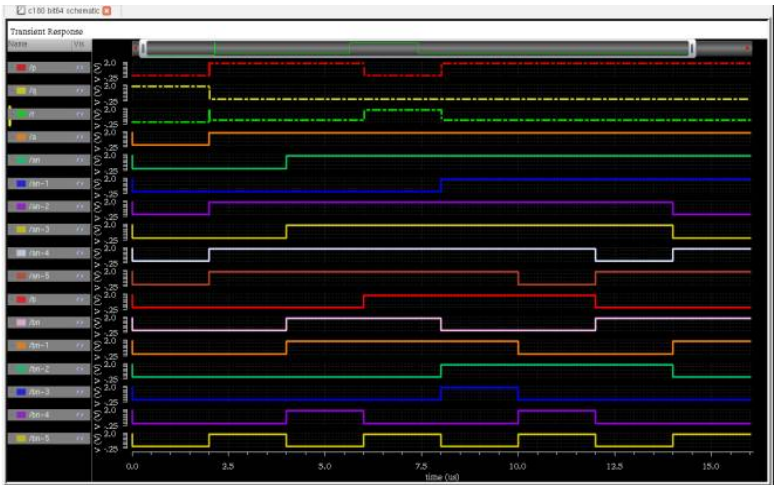

Figure 9: Simulation results of 64-bit reversible comparator

The power and delay of the circuit is calculated using Cadence Virtuoso ADE tool . Figure 10 shows the comparison of delay and power between 64 bit comparator implemented in CMOS logic and reversible logic using GDI (in 45nm technology). also shows the comparison of delay and power between 64 bit comparator implemented in reversible logic using GDI using 45nm and 180nm technologies.

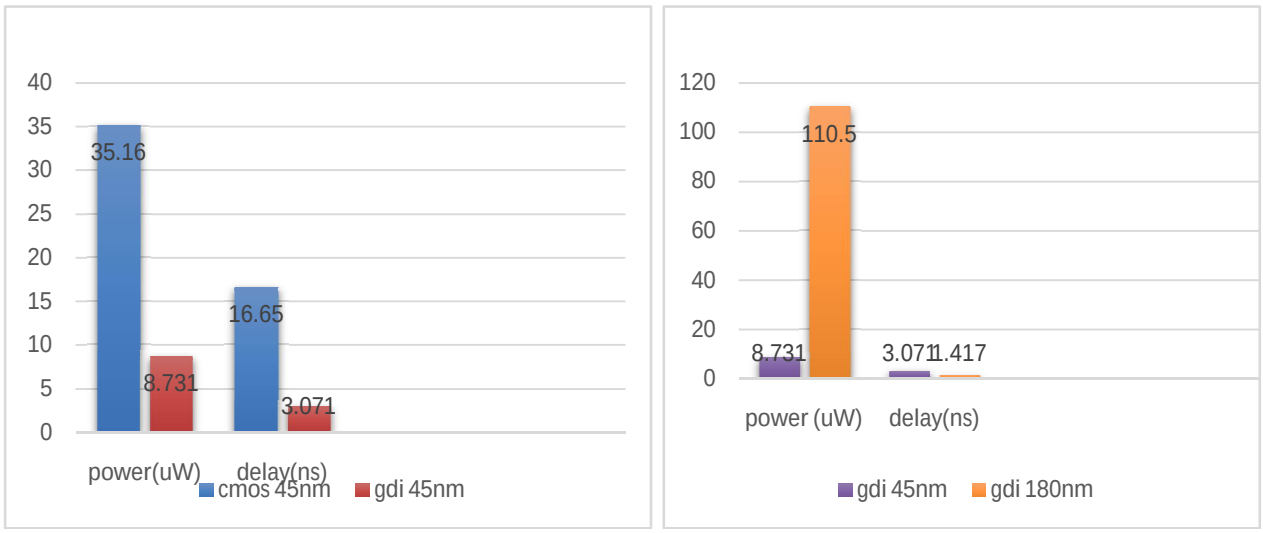

Figure 10: Comparison of power and delay between CMOS and reversible logic

IV. CONCLUSION

In this paper,64 bit comparator with less power consumption, less gates and high speed design is implemented. When implemented in CMOS 45nm technology, the power dissipated is 35.1 microwatts and the delay is 16.65 nanoseconds. The GDI logic is used to decrease the area and power consumption. Using reversible logic along with GDI logic has

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reduced the delay and power significantly. Implementing the Reversible logic along with GDI in 45nm technology has reduced both the power and delay significantly.

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