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A High-Speed Ring Oscillator Operating at Low Voltage Using a IGZO TFTs

Manohar Tammineni, Balaji Singavarapu

Students, Department of Electronics and Communication Engineering, GMR Institute of Technology, Rajam, A.P. India

ABSTRACT: A new high-speed ring oscillator (RO) utilizing amorphous Indium-Gallium-Zinc-Oxide Thin-Film Transistors (a-IGZO TFTs) is presented in this work. By using intermediate signals produced inside the RO, the system reduces single-stage inverter latency and increases speed. The suggested RO was manufactured at 180°C to verify its performance, and it was contrasted with two traditional designs: one that used a bootstrapped pseudo-CMOS inverter and the other that used a diode-load inverter. According to experimental data, at a 6 V supply voltage, the suggested RO produced a frequency of 173.2 kHz and a power-delay-product (PDP) of 0.7 nJ. With frequency increases of 155% and 44% and PDP decreases of 14% and 24.5%, respectively, these outcomes show a notable improvement over the diode-load and pseudo-CMOS solutions. This RO works well with high-speed, low-voltage uses, especially in the creation of timing signals.

KEYWORDS: low-power designs, timing signal generation, oxide thin-film transistors, and high-speed ring oscillators.

I.INTRODUCTION

When comparing Amorphous Indium-Gallium-Zinc-Oxide (a-IGZO) Thin Film Transistor (TFT) technology with alternatives like organic and amorphous silicon (a-Si: H) TFTs, several advantages emerge. These benefits have led to its increasing application in various fields, including radiation detection systems, biosensors, RFID tags, and high-resolution display drivers. However, performance at higher operating frequencies in the MHz range is constrained by factors such as moderate carrier mobility (approximately 10-20 cm^2/Vs) and the absence of a stable, repeatable p-type oxide TFT technology that is compatible with effective CMOS topologies. To address these limitations and enhance performance, circuit-level optimization techniques have been developed, avoiding the need for complex structures (like self-aligned or dual-gate devices) or miniaturized transistors, which would significantly increase production costs.

Ring oscillators (ROs), commonly used as on-chip clock generators, are gaining attention for applications requiring clock frequencies between kilohertz and megahertz, such as NFC systems, wearable health monitoring devices, and smart packaging. Literature has documented several oxide TFT-based ROs that operate in the hundreds of kilohertz range. However, these designs often rely on less stable oxide semiconductors (such as IZO instead of IGZO), double-gate architectures, short channel lengths (less than 10 µm), high supply voltages (greater than 15 V), or combinations of these factors. Although some designs function at lower supply voltages (below 4 V), they typically involve trade-offs. For instance, one approach employs self-aligned structures and pseudo-CMOS inverters but requires two supply voltages for rail-to-rail operation. Another RO design utilizes MESFETs and Schottky diodes but necessitates both positive and negative supply voltages, along with additional processing steps.

This study proposes a cost-effective alternative by employing circuit-level design strategies to enhance performance without altering the device's structure, materials, fabrication methods, or requiring additional supply voltage sources. To tackle these challenges, the proposed high-speed RO architecture leverages intermediate signals generated within the oscillator to minimize inverter stage delay, thereby achieving a high oscillation frequency at low supply voltage (VDD). This approach makes it particularly suitable for the intended applications.

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II. DEVICE FABRICATION AND CHARACTERISTICS:

Oxide TFT circuits were fabricated on glass substrates by a method that is comparable to one detailed in [27]. The devices have a staggered bottom-gate and top-contact morphology, as depicted in the inset of Fig. 1(a). The material stack employed for the device is as follows: sputtered materials consist of molybdenum (Mo) electrodes, Ta_2O_5 and SiO_2 high-k dielectric, and a-IGZO semiconductor with an atomic composition ratio of In:Ga:Zn as 2:1:1.

Circuit interconnections are implemented using an additional Mo layer positioned on top of the TFT

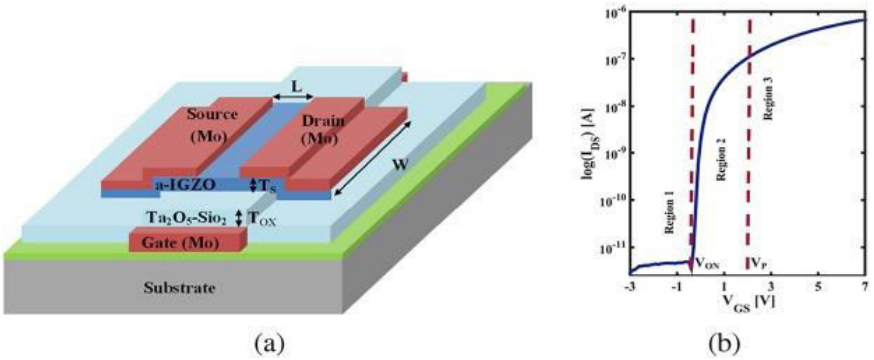

Figure 1: Internal layout diagram and simulation

stack. The use of a low-k Parylene-C interlevel insulator reduces parasitic capacitance. Chemical vapor deposition is used in the formation of the Parylene-C layer, and it will provide both insulation and passivation for the TFTs. Optical lithography and etching are used in defining and patterning the layers. Finally, annealing is performed on the hot plate at 180°C for one hour to complete the fabrication process. Fig. 1 shows the electrical performance of the a-IGZO TFTs, which have channel dimensions of 40 µm width and 10 µm length. These transistors show:

- A turn-on voltage near 0 V,
- An On-Off current ratio exceeding 10^8, and
- A saturation mobility of 25.7 cm^2/Vs.

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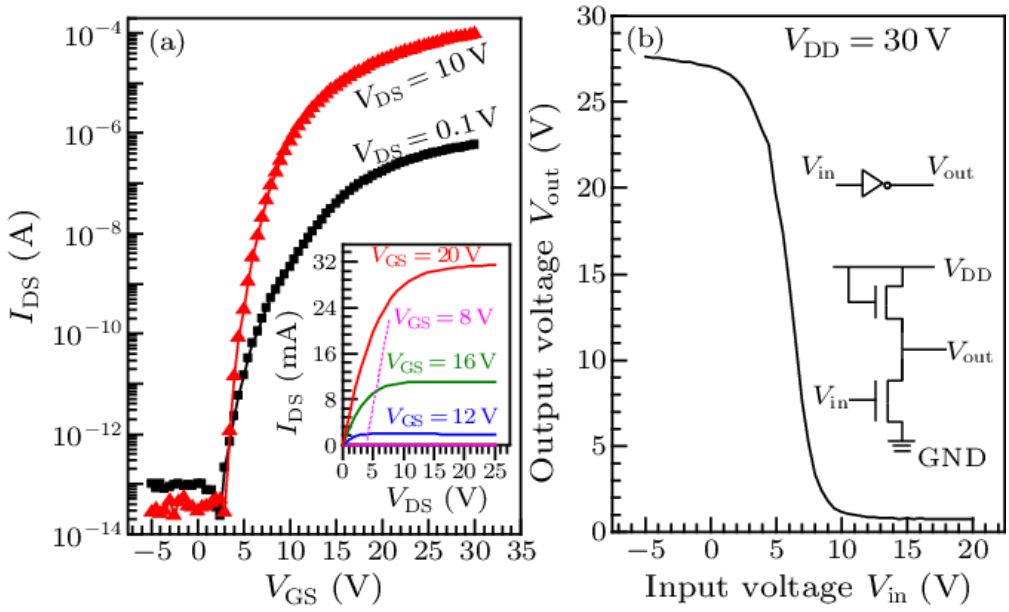
III. HIGH-SPEED RING OSCILLATOR DESIGN



The schematic of the i-th stage inverter of a conventional bootstrapped pseudo-CMOS inverter-based Ring Oscillator (RO) is shown in Fig. 2(a). In this structure, for an n-stage RO, i ranges from 1 to n, and the first stage accepts input from the nth-stage output. The operation of M2 in the bootstrapped pseudo-CMOS inverter is governed by a diode-load inverter, which introduces a propagation delay (td), as shown in Fig. 2(a).

Figure 2: Measured Electrical Characteristics of IGZO TFT with a Channel Width and Length: (a) Transfer Characteristics at a Drain Voltage with the Device Cross-Sectional Schematic in the Inset, and (b) Output Characteristics with Gate Voltage Swept from 0 to 10 V in 0.5 V Increments."

This delay introduces a delay of td on the signal at node b from the signal at node a, which in turn, increases the overall delay in the inverter stage. The oscillation frequency in the RO is inversely related to the delay of one stage inverter. Therefore, the delay td places an upper limit on the operating frequency of the oscillator.

To overcome this limitation, the high-speed RO design uses a bootstrapped pseudo-CMOS inverter stage with gates of M1 and M4 separated, as presented in Fig. 2(b). In the proposed design, the gates of M1 and M4 are separated. The gate of M1, node y is connected to the output of the (i-1)-stage inverter as is conventional for the RO design. However, the signals at the gates of M1 and M4 should be nearly in phase for the circuit to work properly. Moreover, the times at which the signal and its inverted form arrive at nodes y and b, respectively, should coincide. In order to obtain this coincidence, the gate of M4 is connected to the output of the (i-3)-stage inverter or to the (n-(i-3))-stage if i is less than 3. This adjustment ensures the signal arriving at the gate of M4 is arriving a little earlier than it does at the gate of M1. The signal consequently arrives almost simultaneously at nodes b and y, effectively nullifying the delay td. An improvement in oscillation frequency is thereby obtained due to this modification.

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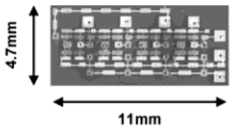
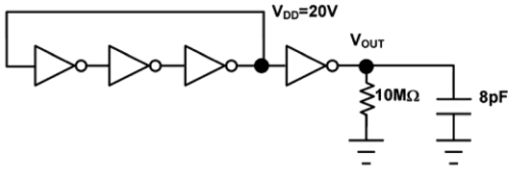
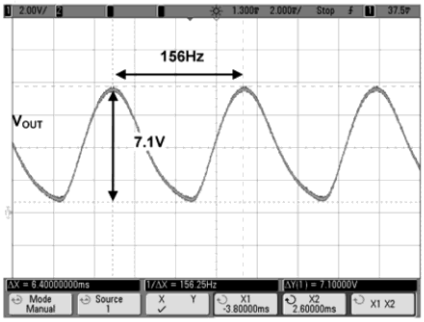




(a)



(b)

Figure 3: Schematic presenting i^{th}-stage inverter

However, unlike the traditional design of Fig. 2(a), in the modified design, the diode-load inverter is It is activated before M1 and M2 are fully operational. Thus, power consumption is slightly greater, but the oscillation frequency significantly increases. Consequently, high-speed RO-based designs exhibit better performance by sacrificing an additional increase in power consumption compared to other conventional approaches.

The schematic and micrograph of a 9-stage proposed RO based on this modified bootstrapped pseudo-CMOS inverter stage are shown in Fig. 3. For comparison, two conventional 9-stage ROs, using the bootstrapped pseudo-CMOS inverter (RO1) and diode-load inverter (RO2), were also fabricated under identical conditions. The micrographs of these conventional ROs are presented in Fig. 4(a) and (b).

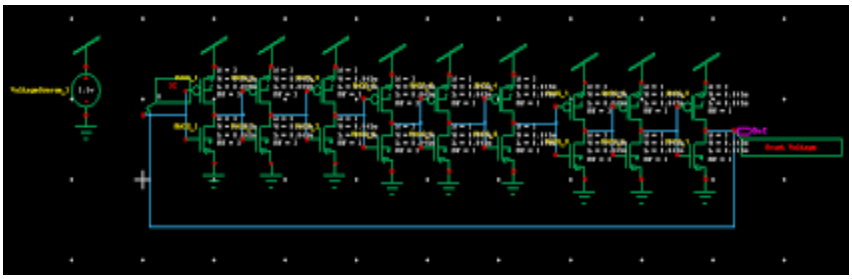


Figure 4: Proposed 9-Stage Ring Oscillator Utilizing a Modified Bootstrapped Pseudo-CMOS Inverter Stage: (a) Schematic Diagram and micrograph

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IV. RESULTS AND DISCUSSIONS

The VTCs of the inverters used in ROs were measured using a probe station. VIN is varied linearly from -5 V to 6 V in 0.1 V steps to get the characteristic. The plot shows nearly rail-to-rail operation of the bootstrapped pseudo-CMOS inverter compared to that of the diode-load inverter, as shown in Fig. 5(a). Fig. 5(b) shows the measurements of ROs at different VDDs of 3 V, 6 V, and 9 V in normal ambient conditions by using Keysight DSOX2002A oscilloscope. The channel length used for these ROs are TFTs of 10 µm. Measured oscillations frequencies of RO1, RO2, and proposed RO at VDD = 6 V are found to be 120 kHz, 68 kHz, and 173.2 kHz, respectively. The suggested RO shows a frequency rise of about 44% (155%) over RO1 (RO2).

The proposed ring oscillator (RO) increases the oscillation frequency with a power consumption that is 15% (113%) more as compared to RO1 and RO2. Performance evaluation of all three ROs is carried out with measured data at various supply voltages, VDD. Performance results are presented in Figures 6(a)-(d). From the plots, it is evident that the proposed RO achieves the highest frequency, the lowest power-delay product (PDP), and the shortest per-stage propagation delay compared to the conventional ROs. However, the voltage swing of the proposed RO is lower compared to RO1. For example, for a 6 V supply, the voltage swing of the proposed RO is 73% of the supply voltage, whereas RO1 reaches 91%. It is worth noting that the experiments were performed without the on-chip output buffers. Therefore, the high load impedance of DSO cables could affect the performance of the RO greatly during measurement. To analyze how the loading condition affects voltage swing, simulations were run at 6 V supply where the swing was plotted for various conditions.

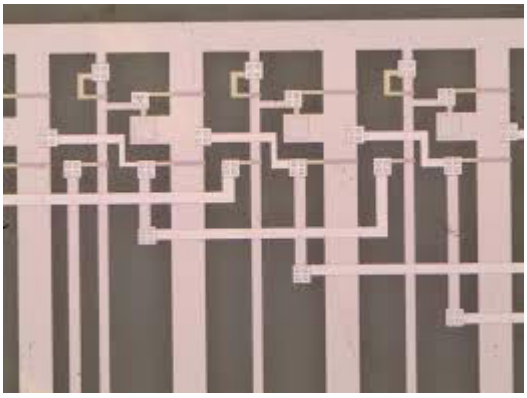

Figure 5: Micrograph of Conventional 9-Stage Ring Oscillators with Bootstrapped Pseudo-CMOS Inverters (RO1) and with Diode-Load Inverters (RO2).

Simulations indicate that for no-load conditions, both RO1 and the proposed RO provide 100% output voltage swing. But with the increase in the impedance of the load, the voltage swing of the proposed RO drops more sharply compared to RO1. The reason behind this is that the output node of the proposed RO acts as an input to two intermediate stages, while in RO1, it acts as an input to just one stage. The degradation in voltage swing propagates through all stages of the RO, leading to a reduced final output voltage swing. However, on-chip output buffers, as implemented in previous works [01]–[03], [04]–[06], would enable the proposed RO to reach nearly full voltage swing and higher oscillation frequencies within a given technology.

Comparing the performance of the designed RO with other ROs extracted from the literature, given in Table I, previous ROs [01]–[02] employed larger supply voltages (≥ 10 V) with restricted voltage swings of under 60% of VDD. Moreover, RO in [05] deployed dual-gate TFTs that add extra fabrication process stages. The TFTs in [06] yielded 40% more mobility as compared to the TFTs in the present study. The RO in [07] uses only simulated results and without parasitic effects due to interconnects. To the contrary, the fabricated RO exhibits a notable improvement in its oscillation frequency, which occurs on a standard device structure, utilizing low supply voltages, all without increasing the complexity associated with their fabrication processes. More so, when employing on-chip output buffers, the suggested RO can enjoy full output voltage swing that is also more efficient as compared to state-of-art designs.

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V. CONCLUSION

Here, a high-speed ring oscillator (RO) using a-IGZO TFTs operating at low supply voltages is presented. The output frequency is improved by 44% and 155% as well as the power-delay product is reduced by 24.5% and 14% compared to RO1 and RO2, respectively, with measurements at a 6 V supply voltage. As a result, the proposed RO is suitable for applications such as smart packaging, biomedical wearable devices, NFC, and RFIDs, in which miniaturized or complex transistor designs are not required.

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