ISSN(Online): 2320-9801
ISSN (Print) : 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(A High Impact Factor, Monthly, Peer Reviewed Journal)

Website: www.ijircce.com

Vol. 7, Issue 2, February 2019

7:2 Compresser Using MCM Algorithm Based Fir Filter

U. Rajasekaran [1], P. Mukil Viswa [2], R. Dinagar [2], S. Muthu Sowmiya [2],

Assistance Professor**,** Department of ECE, Builders Engineering College, Tirupur, Tamilnadu, India[1]

Students. Department of ECE, Builders Engineering College, Tirupur, Tamilnadu, India[2]

ABSTRACT: In this project a new implementation of 7:1 compressor is proposed to be used for fast multiplication or multiple addition applications.The proposed 7:1 compressor and the most efficient contender have been simulated using MODELSIM software. This paper presents a new high speed, low power 7-1 compressor which is constructed according to a sensible combination of pass transistor logics and static logics. It is constructed of a new 5-4 arithmetic block, two 3-2 counters and one 2-1 EXOR. Multiplying filter coefficient with constant number and store it inMCM and it adding each bit with MCM.Therefore, a decrease of gate level delays is achieved which lowers its power dissipation.

KEYWORDS: 7-1 Compressor, High speed, Area Efficient, Pass transistor logic, 5-4 arithmetic block

I. INTRODUCTION

Among different arithmetic blocks, the multiplier is one of the main blocks, which is widely used in different applications especially signal processing applications.

There are two generalarchitectures for the multipliers, which are sequential and parallel. While sequential architectures are low power, their latency is very large. Compressors are one of the critical components of multiplier circuits that are being widely utilized in high speed systems such as digital image processing. Multiplication is basically a two-step process, consisting of formation of partial products followed by the accumulation stage. Since the power consumption and speed are critical parameters in the design of digital circuits, the optimizations of these parameters for multipliers become critically important. Specifically,achieving the desired performance (speed) considering the limited power budget of portable systems is challenging task. In addition, having a given level of reliability may be another obstacle in reaching the system target performance. To meet the power and speed specifications, a variety of methods at different design abstraction levels have been suggested. Approximate computing approaches are based on achieving the target specifications at the cost of reducing the computation accuracy. The FIR filter can be roughly divided into two parts: the first part stores the coefficients in look-up tables (LUTs) in advance; the second part adds the outputs of these LUTs and calculates the final FIR filter output using an adder tree.

II. PREVIOUS WORKS

They proposed four 4:2 compressors, which have the flexibility of switching between the exact and approximate operating modes. In the approximate mode, these dual-quality compressors provide higher speeds and lower power consumptions at the cost of lower accuracy. Each of these compressors has its own level of accuracy in the approximate mode as well as different delays and power dissipations in the approximate and exact modes. Using these compressors in the structures of parallel multipliers provides configurable multipliers whose accuracies (as well as their powers and speeds) may change dynamically during the runtime. The efficiencies of these compressors in a 32-bit Dadda multiplier are evaluated in a 45-nm standard CMOS technology by comparing their parameters with those of the state-of-the-art approximate multipliers

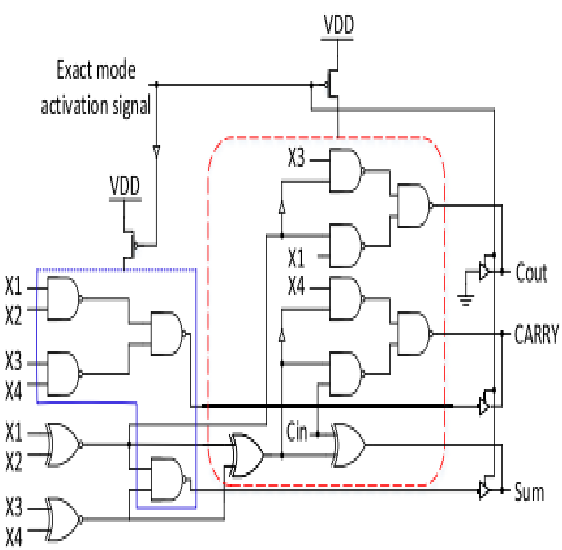
ISSN(Online): 2320-9801
ISSN (Print) : 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(A High Impact Factor, Monthly, Peer Reviewed Journal)

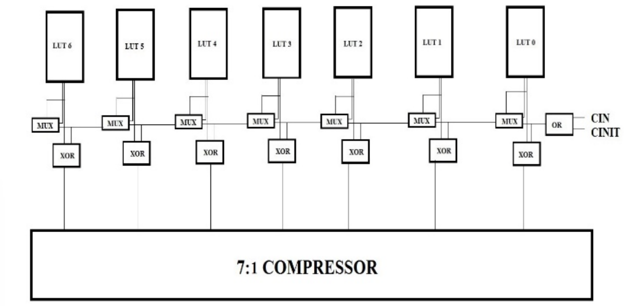
Website: www.ijircce.com

Vol. 7, Issue 2, February 2019



III. DESIGN OF A NEW 7:1 COMPRESSOR

In this project a new implementation of 7:1compressor is proposed to be used for fast multiplication or multiple addition applications. The proposed 7:1compressor and the most efficient contender have been simulated using MODELSIM software.



The filter coefficients are initialized which is get from the filter coefficient i.e. the coefficient is Multiplying filter coefficient with constant number and store it in MCMAdding each bit with MCM Compressing itby7:2compressor. Finally, filtering is done.

IV. FLOW OF DATA

First the filter coefficient is got from the LUT which is stored in the physical memory and that systems is then multiplied with the constant system to get the encoding processes which is then added with the adding system to get through the compression. Adder is the vital role to play the compression processes. After this adder tree compressor, it

ISSN(Online): 2320-9801
ISSN (Print) : 2320-9798

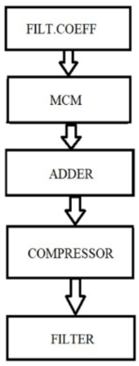
International Journal of Innovative Research in Computer and Communication Engineering

(A High Impact Factor, Monthly, Peer Reviewed Journal)

Website: www.ijircce.com

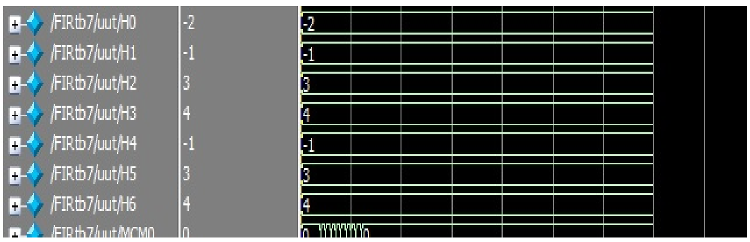
Vol. 7, Issue 2, February 2019

can be sent to the filter for getting a noiseless output on the compressor. On the other hand one can do the systematic view of decompressor to get through the system views.



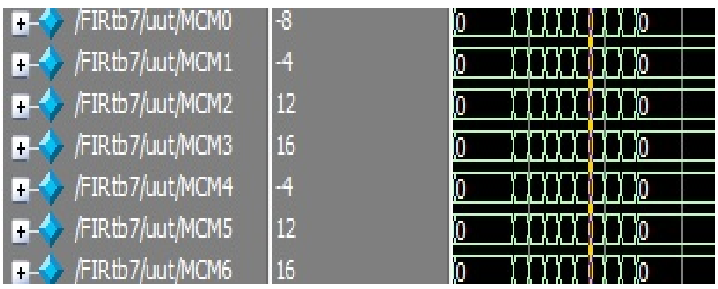
V. MODEL SIMULATION

Model simulation is used in this project to get through the VHDL coding to get the simulation result to get the compression outputs. The program is based on many major proceedings systems to get through the procedure pattern on the titular basises. The sample output and the model system to get through the simulation on the pulse simulation systems. The adder system also encoded in the VHDL coding to get the compressed one. VHDL is used in this purpose because of the user-friendly purposes.



VI. FILTER COEFFICIENT IN LUT

Since the filter coefficient is constant value. It was given as the first input in this program. This constant filter coefficient is taken from the look up table of the memory for the further compression purpose. Here it is denoted in the terms of H1 to H6.



ISSN(Online): 2320-9801
ISSN (Print) : 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

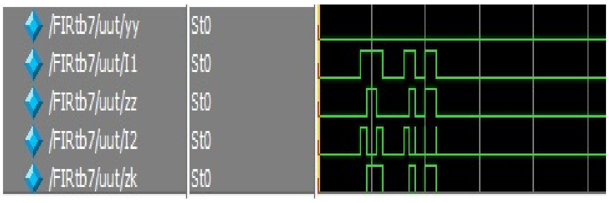
(A High Impact Factor, Monthly, Peer Reviewed Journal)

Website: www.ijircce.com

Vol. 7, Issue 2, February 2019

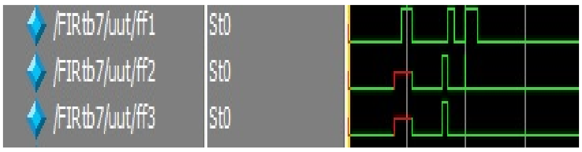
MCM Algorithm:

Multiple constant multiplier is used to reduce the adder requirements in the systematic functioning. Since the input values are of 7 bits, therefore there is a constant value of 7 bits should be multiplied for each. Hence the term MCM0 to MCM6 is used in the program to reduce the adder requirements and the functioning brassies



Two multiplier and One Adder:

To reduce the 7bit into 5bit processes, two multiplier and one adder is used for each stage. Since this multiplier, adder is collectively called as filters. Filtering processes yields the five-bit output from the 7 input bits.



5 to 3 compression:

This section will allow us to compress the 5 bits into 3 bits by comparision processes in VHDL program. Either greater or lesser will be considered. This will allow us to get the 5:3 compression on the required functional basis.

FULL ADDERoperation:

We know that full adder consists of three input and two output, hence this operation will produce a 3:2 compression and finally an XOR gate is used to bring one bit as the final output on the required functioning.

VII. CONCLUSION

In this work analyzes the designing compressor trees by using different compressor technique 7:1. These are used in different applications such as multipliers, digital signal processing, and hardware accelerators, Image processing. By using these compressor techniques speed can be improved and presents no area overhead, delay can be reduced. Using of 1 bit to share information instead of two bits will reduce the system requirements, flipflops, and memory requirements.

REFERENCES

1.Omid Akbari, MehdiKamal, Ali Afzali-Kusha, and Massoud perdram, 2017.Dual –Quality 4:2 Compressor for Utilizing in Dynamic Accuracy Configurable Multipliers.

2.Xiaoqiang Zhang, Le Tu, Dihu Chen, Yuelai Yuvan, Kan Huang, Zixin Wanssors on,2017.Parallel Distributed Arithmetic FIR Filon Xilinx FPGAster Design Based on 4:2 Compressors on Xilinx FPGAs

ISSN(Online): 2320-9801
ISSN (Print) : 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(A High Impact Factor, Monthly, Peer Reviewed Journal)

Website: www.ijircce.com

Vol. 7, Issue 2, February 2019

3.Dash Anindita, Swetapadma Dash and S.K. Mandal, 2014. Design of Optimized Wallace Tree Multiplier in Cadence,International Journal of Computer Applications (IJCA).
4.Priyatharshne, T.N., L. Raja and A. Vinodhini, 2014. An Optimized Wallace Tree Multiplier using Parallel Prefix Han-Carlson Adder for DSP Processors, International Journal of Advanced Research in Electronics and Communication Engineering (IJARECE), 3(11).
5.Senthil kumar, M and S. Ramani, 2013. FPGA Implementation of digital FIR filter
based on truncated multiplier, IOSR Journal of Electronics and Communication Engineering (IOSR-JECE), pp: 44-49.