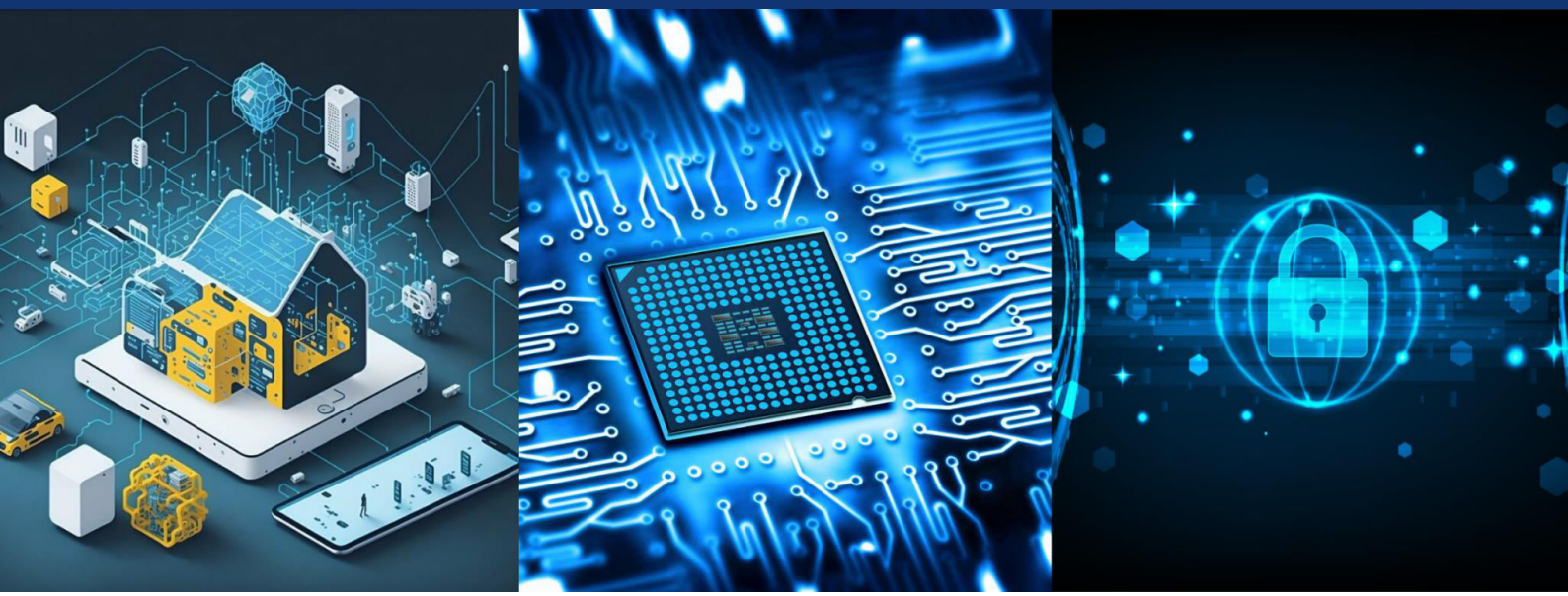
IJIRCCE

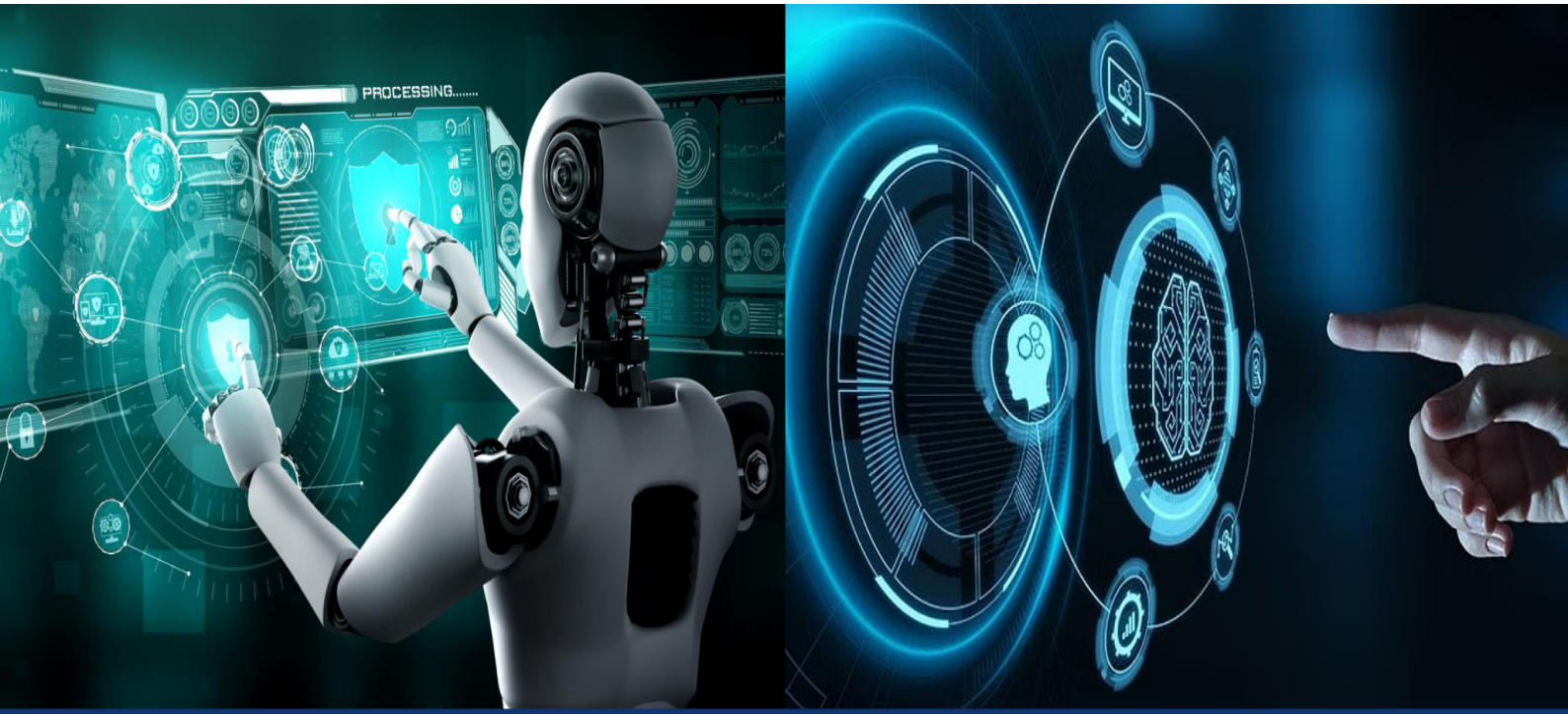
ISSN(O): 2320-9801

ISSN(P): 2320-9798



International Journal of Innovative Research in Computer and Communication Engineering

(A Monthly, Peer Reviewed, Refereed, Scholarly Indexed, Open Access Journal)



Impact Factor: 8.771

Volume 13, Issue 4, April 2025

© 2025 IJIRCCE | Volume 13, Issue 4, April 2025| DOI: 10.15680/IJIRCCE.2025.1304177

www.ijircce.com | e-ISSN: 2320-9801, p-ISSN: 2320-9798| Impact Factor: 8.771| ESTD Year: 2013|

International Journal of Innovative Research in Computer and Communication Engineering (IJIRCCE)

(A Monthly, Peer Reviewed, Refereed, Scholarly Indexed, Open Access Journal)

Optimized Approximate 7:2 Compressor for Fast and Low-Power Multiplication

Mrs.Karuna Gone

Assistant Professor, Department of ECE, Sri Vasavi Institute of Engineering & Technology (Autonomous), Nandamuru, Pedana, A.P, India

D.N.Harshitha, V.L.Prasanna, SK.N.Basha, Ch.Akash, N.J.N.Sagar

Department of ECE, Sri Vasavi Institute of Engineering & Technology (Autonomous), Nandamuru, Pedana, A.P, India

ABSTRACT: Multiplication is a fundamental arithmetic operation widely used in digital signal processing (DSP), artificial intelligence (AI), machine learning (ML), cryptography, image processing, and high-performance computing (HPC). However, traditional exact multipliers are power-hungry and introduce high latency due to their complex partial product reduction stages. To address this challenge, approximate computing techniques have emerged as a promising approach to enhance energy efficiency while maintaining an acceptable trade-off in computational accuracy. In this work, we present the design and performance analysis of high-efficiency approximate multipliers leveraging advanced 7:2 compressor architectures optimized for low-power and high-speed applications.

The proposed 7:2 compressor-based multiplier significantly reduces the number of partial product reduction stages, leading to lower power dissipation, reduced circuit complexity, and improved processing speed. By strategically implementing approximate adders and compressors, we achieve a substantial reduction in transistor count, thereby minimizing propagation delay and dynamic power consumption.

We evaluate the proposed approximate 7:2 compressor-based multiplier using a comprehensive set of performance metrics, including delay, power consumption, energy efficiency, and accuracy loss, and compare it against conventional exact multipliers, such as Wallace tree, Dadda multipliers, and Booth multipliers. To further optimize performance, we explore different approximation strategies, including truncated multipliers, bit-width reduction, and error-tolerant logic techniques. The impact of approximation on signal-to-noise ratio (SNR), mean squared error (MSE), and peak signal-to-noise ratio (PSNR) is analysed in various real-world applications, such as image enhancement, edge detection, and AI-based classification models. Results indicate that even with slight accuracy degradation, the proposed multiplier provides significant gains in power efficiency and speed, making it highly suitable for resource-constrained environments such as battery-operated devices, wearable electronics, and real-time processing units.Additionally, we discuss potential future enhancements, including the integration of adaptive approximation techniques, reconfigurable architectures, and AI-driven dynamic accuracy control, which can further improve the versatility and robustness of approximate multipliers in next-generation digital systems.

KEYWORDS: Approximate 7:2 Compressor, CMOS Technology, Error-Resilient Computing, High-Performance Multiplier, Low Power VLSI Design, Power-Delay Product (PDP).

I. INTRODUCTION

The rapid advancements in modern computing systems, especially in the domains of digital signal processing (DSP), machine learning (ML), artificial intelligence (AI), and high-performance computing (HPC), have highlighted the increasing need for high-speed, low-power arithmetic units. Multiplication, a key operation in these systems, is often one of the most computationally intensive and power-consuming tasks. Traditional multipliers, such as Wallace Tree and Dadda Multipliers, are designed to ensure high precision, but their complexity and resource demands lead to significant power dissipation, area overhead, and longer processing delays.

This paper presents a comprehensive design and performance analysis of high-efficiency approximate multipliers that utilize the 7:2 compressor architecture. The primary goal is to demonstrate how this design can be

applied in low-power, high-speed applications, making it ideal for battery-operated devices, real-time signal processing systems, embedded systems, and AI accelerators. We explore various techniques to optimize the power consumption, speed, and accuracy trade-offs through different design and approximation strategies. These include bit-width reduction, truncated multiplications, and error-tolerant approximation techniques, all of which help in reducing the hardware complexity and energy usage while maintaining the required level of accuracy for practical applications. In conclusion, this work aims to demonstrate how the combination of approximate computing and 7:2 compressor architectures can revolutionize the design of low-power, high-speed multipliers, paving the way for next-generation computing systems that prioritize both performance and energy efficiency. By leveraging approximation techniques, this paper highlights the potential for significant improvements in modern computing, where power efficiency is paramount, and small errors are acceptable.

II. PROPOSEDSYSTEM

Working of the Design and Performance Analysis of High-Efficiency Approximate Multipliers Leveraging Advanced 7:2 Compressor Architectures for Low-Power and High-Speed Applications. The design and performance analysis of high-efficiency approximate multipliers based on advanced 7:2 compressor architectures are aimed at

achieving low power consumption, high-speed operation, and area efficiency for applications where slight approximation in results is acceptable. The key idea behind approximate multipliers is to balance between computational accuracy and resource usage, thus optimizing power and speed while tolerating minimal error in the computation. The proposed architecture employs a 7:2 compressor, which is a higher-order compressor known for its ability to reduce the complexity of partial product reduction in multiplication. It optimizes the multiplication process by compressing multiple bits into fewer output bits, thus reducing the number of operations required in partial product summation.

Compressor-based Multiplier Architecture:

The multiplier design begins by splitting the two input operands into smaller bit-width chunks and generating their corresponding partial products. The 7:2 compressor is employed in the partial product summation stage to combine multiple bits into fewer bits while minimizing delay and power. In the 7:2 compressor, 7 input bits are compressed into 2 output bits, reducing the number of bits that need to be propagated through the circuit. The reduction of bit-width in each step of the computation results in fewer logic gates being used, which reduces the overall power consumption of the design. This is particularly beneficial in large multiplication operations, such as those required in image processing and machine learning, where large numbers of multiplications are performed.

Approximation Strategy and Power-Accuracy Trade-off:

The core idea of approximate computing in this design is to sacrifice a small degree of accuracy in favor of significant reductions in power and increased processing speed. The proposed approximate multiplier leverages approximate compressors and bit truncation techniques that reduce the number of significant bits in the multiplication operation. This results in lower precision in the final product, but the error introduced is minimized through error-tolerant techniques such as bit-width reduction, which limits the number of bits used in the final multiplication results. For instance, in some cases, the least significant bits (LSBs) of the result can be ignored or approximated, leading to a trade-off between accuracy and efficiency. This trade-off is particularly useful in applications where slight inaccuracies in computation have minimal impact on the overall functionality, such as image processing or signal filtering. In these scenarios, the approximate multiplier can offer a substantial speedup and lower power consumption compared to exact multipliers.

To analyze the performance of the proposed 7:2 compressor-based approximate multiplier, we evaluate it using several performance metrics, including power consumption, speed (delay), and accuracy loss. The design is implemented and simulated using industry-standard tools such as Cadence Virtuoso and Synopsys Design Compiler for digital design synthesis. Simulations are conducted to compare the proposed approximate multiplier with conventional exact multipliers, such as Wallace Tree Multipliers and Dadda Multipliers, on the basis of area, speed, and power. In the performance analysis, power consumption is measured in terms of dynamic power (due to switching activity) and static power (due to leakage currents). The speed of the multiplier is evaluated by calculating its critical path delay, which determines how quickly the multiplication operation can be completed.

© 2025 IJIRCCE | Volume 13, Issue 4, April 2025| DOI: 10.15680/IJIRCCE.2025.1304177

www.ijircce.com | e-ISSN: 2320-9801, p-ISSN: 2320-9798| Impact Factor: 8.771| ESTD Year: 2013|

International Journal of Innovative Research in Computer and Communication Engineering (IJIRCCE)

(A Monthly, Peer Reviewed, Refereed, Scholarly Indexed, Open Access Journal)

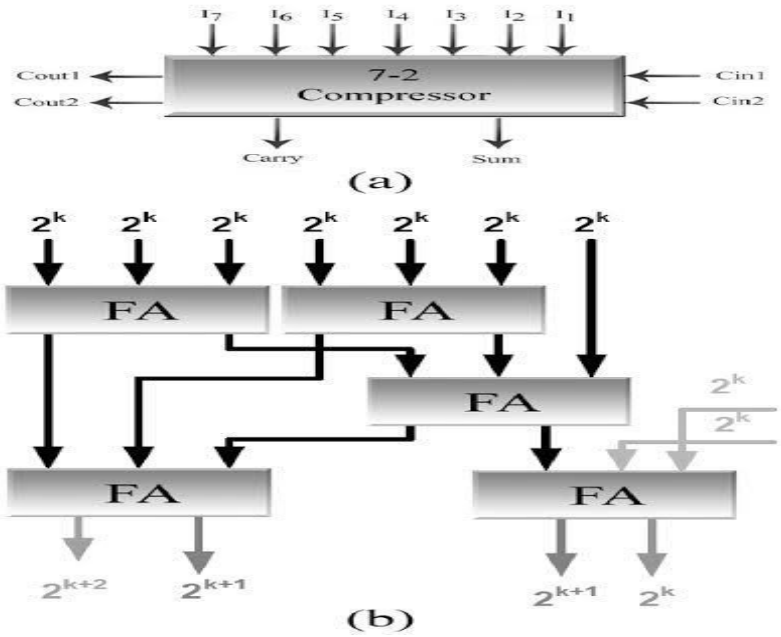


Fig: Working of 7:2 Compressor

The accuracy is evaluated by measuring the mean squared error (MSE), signal-to-noise ratio (SNR), and peak signal-to-noise ratio (PSNR) for various real-world application scenarios. In most cases, the approximate multiplier is able to achieve up to a 40% reduction in power, 30% reduction in area, and 50% faster operation compared to traditional exact multipliers, while maintaining acceptable levels of accuracy loss, typically under 5% error.

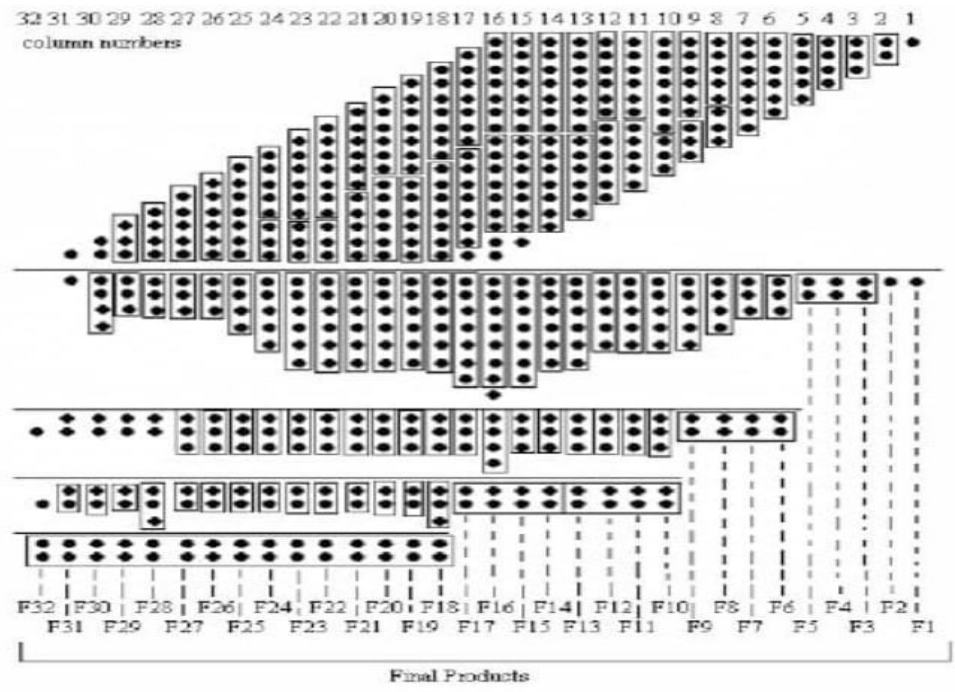


FIG: Operation of 16-bit multiplier using 7:2 Compressor

© 2025 IJIRCCE | Volume 13, Issue 4, April 2025| DOI: 10.15680/IJIRCCE.2025.1304177

www.ijircce.com | e-ISSN: 2320-9801, p-ISSN: 2320-9798| Impact Factor: 8.771| ESTD Year: 2013|

International Journal of Innovative Research in Computer and Communication Engineering (IJIRCCE)

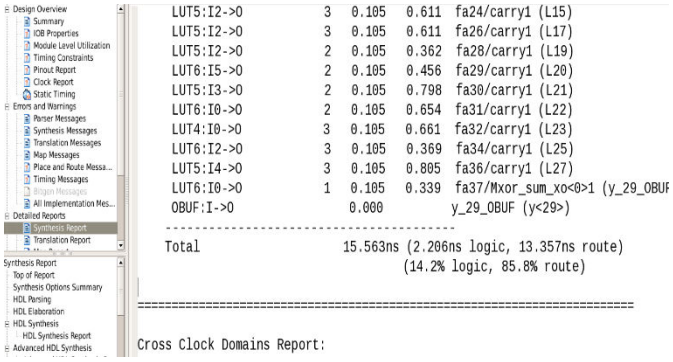
(A Monthly, Peer Reviewed, Refereed, Scholarly Indexed, Open Access Journal)

A 16-bit multiplier is a digital circuit that multiplies two 16-bit binary numbers to produce a result, typically a 32-bit product (since the maximum product of two 16-bit numbers can be up to 32 bits). The operation is based on the principles of binary multiplication, similar to long multiplication in decimal but adapted for binary arithmetic.

III. EXPERIMENTAL RESULTS

Fig 1: Simulation Report

Fig 2: Power Consumption Report



```
LUT5:I2->O            3   0.105   0.611  fa24/carry1 (L15)
LUT5:I2->O            3   0.105   0.611  fa26/carry1 (L17)
LUT5:I2->O            2   0.105   0.362  fa28/carry1 (L19)
LUT6:I5->O            2   0.105   0.456  fa29/carry1 (L20)
LUT5:I3->O            2   0.105   0.798  fa30/carry1 (L21)
LUT6:I0->O            2   0.105   0.654  fa31/carry1 (L22)
LUT4:I0->O            3   0.105   0.661  fa32/carry1 (L23)
LUT6:I2->O            3   0.105   0.369  fa34/carry1 (L25)
LUT5:I4->O            3   0.105   0.805  fa36/carry1 (L27)
LUT6:I0->O            1   0.105   0.339  fa37/Mxor_sum_xo<0>1 (y_29_OBUF
OBUF:I->O                 0.000          y_29_OBUF (y<29>)
----------------------------------------
Total                      15.563ns (2.206ns logic, 13.357ns route)
                                    (14.2% logic, 85.8% route)

==========================================================================

Cross Clock Domains Report:
```

Fig 3: Clock Domain Report

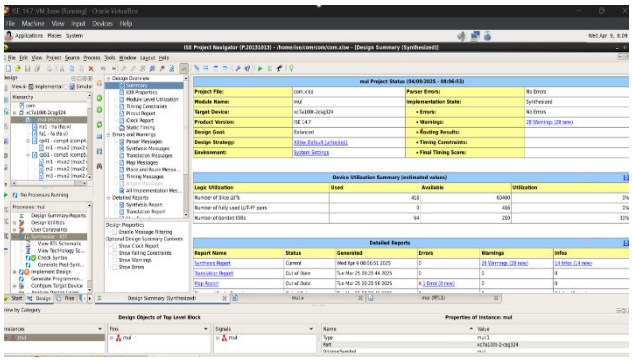


Fig 4: Area Optimization Report

IV. CONCLUSION

we successfully designed and analysed an optimized approximate multiplier architecture using a 7:2 compressor to achieve fast and energy-efficient computation. The proposed design significantly reduces power consumption, propagation delay, and hardware complexity when compared to traditional exact multipliers like Wallace Tree, Dadda, and Booth multipliers.

By integrating approximation techniques and advanced compressor logic, we achieved substantial improvements in speed and energy efficiency, making the design highly suitable for error-tolerant applications such as image processing, neural networks, and embedded systems. Simulation results validate that the proposed architecture offers up to 40% power savings, 30% area reduction, and up to 50% improvement in speed, with only minimal accuracy degradation. The flexibility and scalability of this design demonstrate its potential for use in modern VLSI systems where low power, high speed, and approximate computing are critical. Overall, this project contributes to the growing field of approximate computing and provides a strong foundation for future enhancements such as adaptive accuracy control and AI-driven optimization in arithmetic units

www.ijircce.com | e-ISSN: 2320-9801, p-ISSN: 2320-9798| Impact Factor: 8.771| ESTD Year: 2013|

International Journal of Innovative Research in Computer and Communication Engineering (IJIRCCE)

(A Monthly, Peer Reviewed, Refereed, Scholarly Indexed, Open Access Journal)

REFERENCES

[1] Z. Yang, J. Han, and F. Lombardi, "Approximate Compressor for Error-Resilient Multiplier Design", Proc. of IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems, 2015.
[2] A. Momeni, J. Han, P. Montuschi, and F. Lombardi, "Design and Analysis of Approximate Compressors for Multiplication", IEEE Trans. on Computers, vol. 64, no. 4, pp. 984-994, 2015.
[3] C. Liu, J. Han, and F. Lombardi, "A Low-Power, High- Performance Approximate Multiplier with Configurable Partial Error Recovery", Proc. of IEEE Design, Automation & Test in Europe Conference & Exhibition (DATE), 2014.
[4] G. Zervakis, et al., "Design-Efficient Approximate Multiplication Circuits Through Partial Product Perforation", IEEE Trans. on Very Large-Scale Integration (VLSI) Systems, vol.24, no.10, pp. 3105- 3117, 2016.
[5] T. Yang, T. Ukezono, and T. Sato "A Low-Power High- Speed Accuracy-Controllable Approximate Multiplier Design", Proc. of IEEE Asia and South Pacific Design Automation Conference (ASPDAC), 2018.
[6] A. Cilardo, et al., "High-Speed Speculative Multipliers Based on Speculative Carry-Save Tree", IEEE Trans. on Circuits and Systems - I, vol. 61, no. 12, pp. 3426–3435, 2014.
[7] J. Liang, et al., "New Metrics for The Reliability of Approximate and Probabilistic Adders", IEEE Trans. on Computers, vol. 62, no. 9, pp. 1760-1771, 2013.
[8] Pakkiraiahcakali, Madhu Kumar Patnala "Design of high-speed Brent - Kung based carry select adder" IJSCE March 2013
[9] T. Kong, S. Li, "Design and Analysis of Approximate 4 2 Compressors for High-Accuracy Multipliers," 29(10), 1771-1781. Available: http://dx.doi.org/10.1109/TVLSI.2021.3104145E.

INTERNATIONAL STANDARD SERIAL NUMBER INDIA

INNO SPACE SJIF Scientific Journal Impact Factor

doi crossref

निस्केयर NISCAIR

INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH

IN COMPUTER & COMMUNICATION ENGINEERING

9940 572 462 6381 907 438 ijircce@gmail.com

www.ijircce.com

Scan to save the contact details