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A Low Power Timing Error Tollerant Circuit by Controlling a Clock

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ABSTRACT: This project presents clock controlling technique in flip flops to prevent timing errors. Timing errors are detected and corrected by modify the clock of flip flop without changing the system clock with minimum logics. Timing error is now getting increased attention due to the high rate of error-occurrence on semiconductors. Even slight external disturbance can threaten the timing margin between successive clocks since the latest semiconductor operates with high frequency and small supply voltage. To deal with a timing error, many techniques have been introduced. Nevertheless, existing methods that mitigate a timing error mostly have time-delaying mechanisms and too complex operation, resulting in a timing problem on clock-based systems and hardware overhead. In this article, we propose a novel timing-error-tolerant method that can correct a timing error instantly through a simple mechanism. By modifying a clock in a flip-flop, the proposed system can recover a timing error without the loss of time in the clock-based system. Furthermore, due to the compact mechanism, the proposed system has low hardware overhead in comparison with existing timing-error-tolerant systems that can recover the error instantly. This paper analyses the operating principles of Timing error tolerant circuit and also the proposed system with Time Borrowing concept. To analyse this paper, it is necessary to know some basic terminology such as Error detection and correction, fault tolerant systems, soft error, timing error tolerant system, timing error

KEYWORDS: Very large-scale integration, Latch with time-borrowing detection, Error-detection sequential

I. INTRODUCTION

In modern manometer-scale integrated circuits, timing errors have become a critical reliability issue due to increasing complexity and the use of multi-voltage and multi-frequency designs. Variations in CMOS processes, power supply, and temperature, along with transistor aging effects such as Negative-Bias Temperature Instability (NBTI), further exacerbate the likelihood of timing errors, especially in circuits operating near their performance limits. Traditional design approaches rely on adding safety margins, such as lower clock frequencies or higher supply voltages, to mitigate these errors. However, this often results in performance degradation and increased power consumption. This paper presents a novel technique for detecting and correcting timing errors using a **bit-flipping flip-flop** design. By complementing the output of a flip-flop when an error is detected, this method improves system reliability while reducing performance penalties. In addition, **time borrowing** techniques allow the redistribution of timing slack across pipeline stages, enabling the system to operate at clock periods shorter than the critical path delay with minimal performance overhead. The combination of error detection, correction, and time borrowing offers an efficient solution to address timing variations and enhance the robustness of integrated circuits, even under worst-case process, voltage, and temperature conditions. The proposed methodology aims to improve tolerance to delay variations in logic circuits with minimal impact on performance and energy efficiency, making it a promising approach for future high-speed, low-power digital systems.

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II. RELATED WORK

M. R. Choudhury, V. Chandra, R. C. Aitken and K. Mohanram, "Time Borrow in Circuit Designs and Hardware Prototyping for Timing Error Resilience," in IEEE Transactions on Computers, vol. 63, no. 2, pp. 497-509, Feb. 2014.[6]As dynamic variability increases with CMOS scaling, it is essential to incorporate large design time timing margins to ensure yield and reliable operation. Online techniques for timing error resilience help recover timing margins, improving performance and/or power consumption. This paper presents TIMBER, a technique for online timing error resilience that masks timing errors by borrowing time from successive pipeline stages. TIMBER-based error masking can recover timing margins without instruction replay or roll-back support. Three sequential circuit elements are described: TIMBER flip-flop, dedicated TIMBER flip-flop, and TIMBER latch. The TIMBER flip-flop uses two master latches and one slave latch to mask timing errors by borrowing discrete units of time from successive pipeline stages. It can be simplified to a dedicated TIMBER flip-flop that uses only two latches for time borrowing (TB) at the expense of the flexibility of configuration as a conventional master-slave flip-flop. The TIMBER latch masks timing errors through continuous time-borrowing from successive pipeline stages, and supports runtime configuration as a conventional master-slave flip-flop. The TIMBER latch's continuous time-borrowing capability provides better time-borrowing capabilities at lower hardware cost, but the TIMBER flip-flop's discrete time-borrowing capability preserves the edge triggering property of a flipflop, thus blocking the propagation of glitches and spurious transitions. In addition to evaluating the overhead and trade-offs of TIMBER-based error masking on an industrial processor, the three circuits were also prototyped on an FPGA and their timing error masking capability was validated using a two-stage pipeline test structure. Summary: From the analysis of this paper, this system corrects a timing error by borrowing time from the next pipeline stage, the whole system is not delayed for the recovery of a timing error.

M. Seok, G. Chen, S. Hanson, M. Wieckowski, D. Blaauw and D. Sylvester, "CAS-FEST 2010: Mitigating Variability in Near-Threshold Computing," 18 in IEEE Journal on Emerging and Selected Topics in Circuits and Systems, vol. 1, no. 1, pp. 42-49, March 2011.[1] Near threshold computing has recently gained significant interest due to its potential to address the prohibitive increase of power consumption in a wide spectrum of modern VLSI circuits. This tutorial paper starts by reviewing the benefits and challenges of near threshold computing. We focus on the challenge of variability and discuss circuit and architecture solutions tailored to three different circuit fabrics: logic, memory, and clock distribution. Soft-edge clocking, body biasing, mismatch-tolerant memories, asynchronous operation and low-skew clock networks are presented to mitigate variability in the near threshold V DD register. Summary: Due to the negative-bias temperature instability (NBTI) in CMOS, the threshold voltage is lowered, which finally increases the path delays of logics is studied. M. Ahmadi, B. Alizadeh and B. Forouzandeh, "A Timing Error Mitigation Technique for High Performance Designs," 2015 IEEE Computer Society Annual Symposium on VLSI, 2015, pp. 428-433.[11] Dynamic flip-flop conversion (DFFC) is a time borrowing method which converts the critical flipflops into transparent latches to allow timing slacks pass between pipeline stages of given circuits. However, our previous DFFC methods [13] [14] suffer from false error prediction. It means even when there is no setup time violation, our previous method incorrectly issues timing errorIn this paper we present an improved DFFC method which consumes less power and unlike previous DFFC methods does not suffer from false errors. Also, we investigate the effectiveness of our proposed DFFC method on different benchmarks by considering all existing critical paths, instead of applying our method only to one of critical paths as done in. Summary: In this project, the system can avoid the penalty of the clock but it requires a large amount of hardware, such as an additional flip-flop and latch. Furthermore, since the location of the halfway of the combinational circuits is inaccurate and it is hard to be chosen.

S. Valadimas, A. Floros, Y. Tsiatouhas, A. Arapoyanni and X. Kavousianos, "The Time Dilation Technique for Timing Error Tolerance," in IEEE Transactions on Computers, vol. 63, no. 5, pp. 1277-1286, May 2014.[5] Timing error tolerance is of great importance in nanometre technology integrated circuits. In this paper, 19 the Time Dilation design technique is proposed that provides concurrent error detection and correction in the field of application and also supports off-line manufacturing scan testing. By utilizing a new scan Flip-Flop, the Time Dilation technique is capable to detect and correct multiple errors at the minimum penalty of one clock cycle delay. The silicon area overhead and the power consumption are substantially reduced, as compared to the Razor design approach, since no additional memory elements are required. At the same time, the proposed technique introduces only negligible performance degradation since no extra circuitry is inserted in the critical paths of a design. Summary: From this paper, we understand that in error detection and correction system, they compare an input of a flip-flop and an output of a flip-

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flop with an XOR gate. By using XOR gates and memory elements, the output is corrected when a fault signal is flagged. Since the time interval is required for the error detection and correction, they return to the normal operation after one clock is sacrificed for the recovery

III. PROPOSED ALGORITHM

****3.1 Existing System****

Time borrowing, a widely-used technique in high-performance digital circuits, allows logic stages in a pipeline to automatically borrow time from subsequent cycles or utilize slack from previous cycles without requiring additional circuitry or clock adjustments. In this approach, latches—being level-sensitive—can capture and propagate data over a range of times during their transparent period, enabling higher flexibility than edge-triggered flip-flops in terms of achieving shorter clock periods. This mechanism is particularly effective in reducing clock skew and jitter while optimizing the performance of critical delay paths in high-speed circuits, such as adders.

The technique, also known as cycle stealing, leverages the level-sensitive nature of latches to extend the valid signal transition period beyond the clock edge, allowing the propagation of correct values to the next stage. Time-borrowing latches, especially pulsed latches with time-borrowing detection (LTD), are deployed in critical paths, where they detect and compensate for delay variations caused by process, voltage, and temperature (PVT) fluctuations. These latches, in combination with clock-shifting techniques, stretch the clock period to prevent timing errors while maintaining system functionality without adjusting supply voltage or clock frequency.

Replica-based circuits have been used for variation compensation by dynamically adjusting the supply voltage or clock frequency upon detecting delay errors. However, these methods suffer from limitations due to geographical mismatches between the replica and actual circuits, requiring additional safety margins. In contrast, in-situ error detection mechanisms, such as Razor, use shadow latches to detect timing errors and enable recovery by stalling the pipeline. While effective, these methods introduce performance penalties, especially in high-activation critical paths.

The proposed system extends the concept of time borrowing and clock stretching to minimize timing errors in critical paths. By utilizing pulsed latches, the design eliminates the need for multiple clocks and minimizes performance penalties associated with clock-gating or architectural replay methods. This approach enhances system performance and reliability by tolerating dynamic variations in logic stage delays while maintaining minimal overhead

****3.2 Proposed System****

This paper presents a novel timing-error-tolerant method capable of immediate error correction through a simple mechanism. The system detects abnormal data transitions in critical paths caused by timing errors and corrects them by controlling the transparent window of the clock, ensuring the minimum number of logic elements are used for error resolution. In cases where consecutive timing errors occur across multiple stages, the system's modified clock in the second stage extends the transparent window, allowing normal data to be stored without altering the system clock.

The proposed system consists of two key components: a **transition detector** and a **master clock generator**. The transition detector identifies input transitions at the flip-flop and generates an error-flagged pulse. This signal is then processed by the master clock generator, which creates a pulse that extends the clock’s transparent window, allowing the flip-flop to pass the correct data, even if delayed. This mechanism ensures timing errors are corrected while maintaining the flip-flop’s functionality.

The internal structure of the transition detector comprises an inverter, buffers, and AND gates, designed to detect transitions in both low-to-high and high-to-low states. Upon detecting a transition error, the signal is sent to the master clock generator, which consists of an OR gate and inverter to generate the necessary pulse. This pulse keeps the clock of the master latch (CM) high for a specific period, ensuring the delayed normal data is stored in the flip-flop, correcting the erroneous output.

In cases where timing errors persist across successive stages, the proposed system employs a **time-borrowing** technique. If a second-stage flip-flop encounters a timing error due to setup-time violations, the system extends the

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transparent window of the clock in the second stage by adjusting the delayed clock (CLKDD). This enables the delayed data to be stored correctly, preventing data loss. The time-borrowing circuit structure includes logic gates that maintain the correct signal transition and ensure the system can handle errors at any stage where setup time is insufficient.

In summary, this proposed system improves timing-error resilience by detecting and correcting errors in real-time through minimal logic intervention. It extends the transparent window during timing errors, employs time-borrowing for successive errors, and ensures high system performance without requiring changes to the clock frequency or supply voltage.

IV. SIMULATION RESULTS

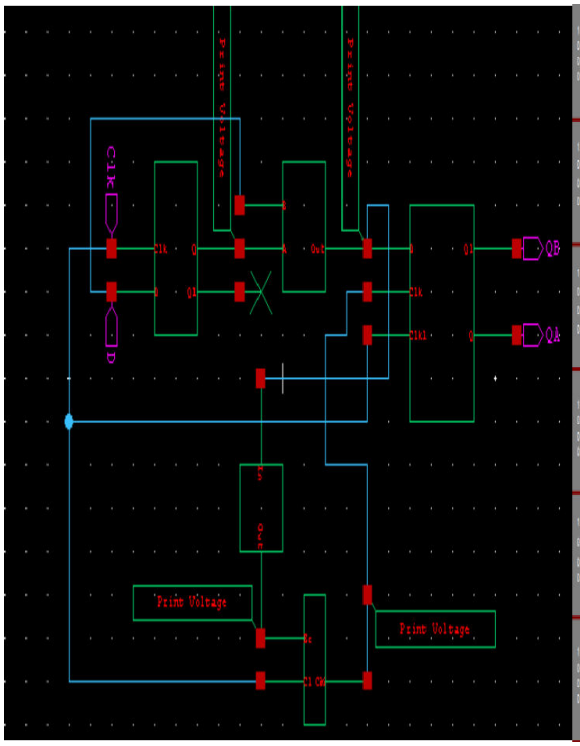

Fig 1: Schematic of Timing error tolerant circuit

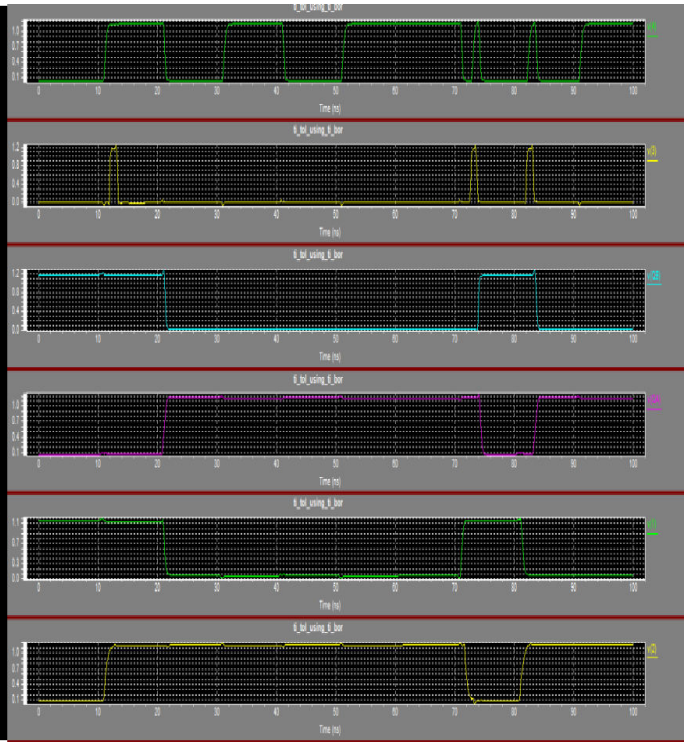

Fig 2 : Output for Timing error tolerant circuit

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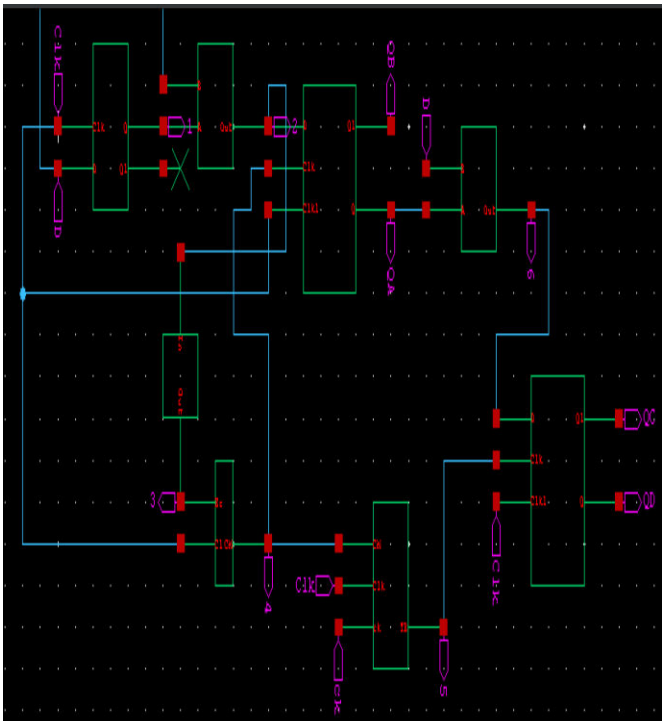
Fig 3: Schematic of Timing error tolerant circuit using Time Borrow Technique.



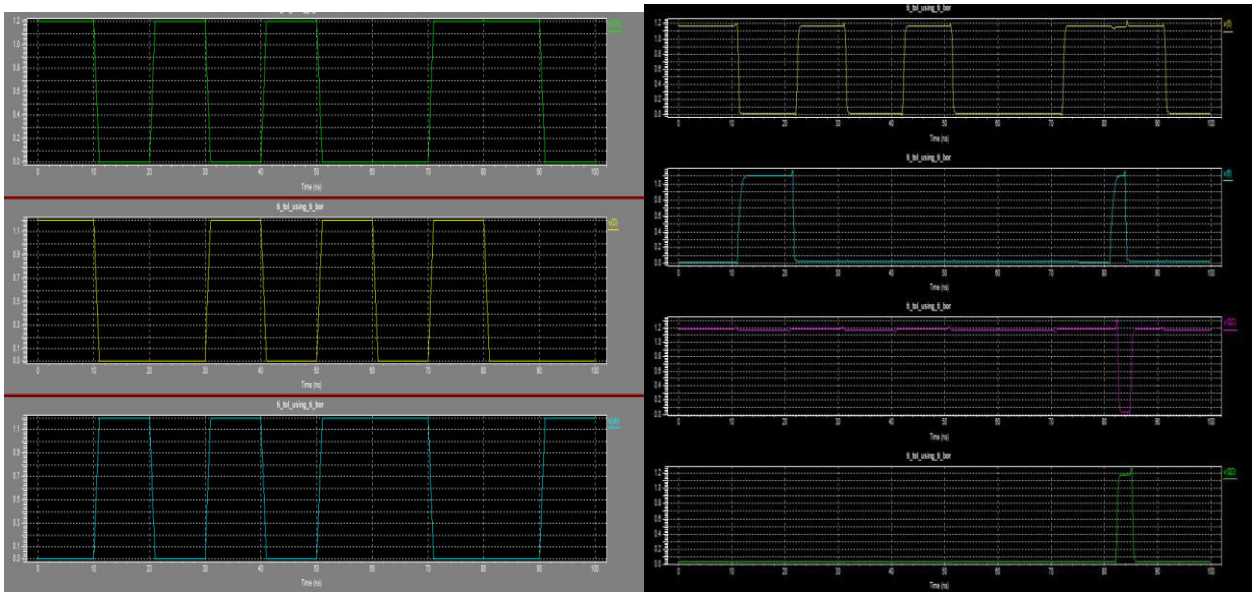


Fig 4: Inputs and Outputs for the Timing error tolerant circuit with Time Borrow Technique

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V. CONCLUSION AND FUTURE WORK

FUTURE SCOPE Our proposed system is designed to operate the targeted function, but it is not yet designed with consideration for possible glitches. Since the glitch occurs for a short duration, the glitch can be removed by adjusting CMOS parameters. For instance, if the width or the length of transistors in the "transition detector" is changed, the glitch can be removed by adjusting the rising or falling slope. With this technique, signal "Er" could be delayed, which can result in a little lower performance. On the other way, the glitch can be removed by changing the circuit of the "transition detector," which could cause larger hardware overhead. To address the glitch, we can adopt one of the methods that are stated above in further study

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