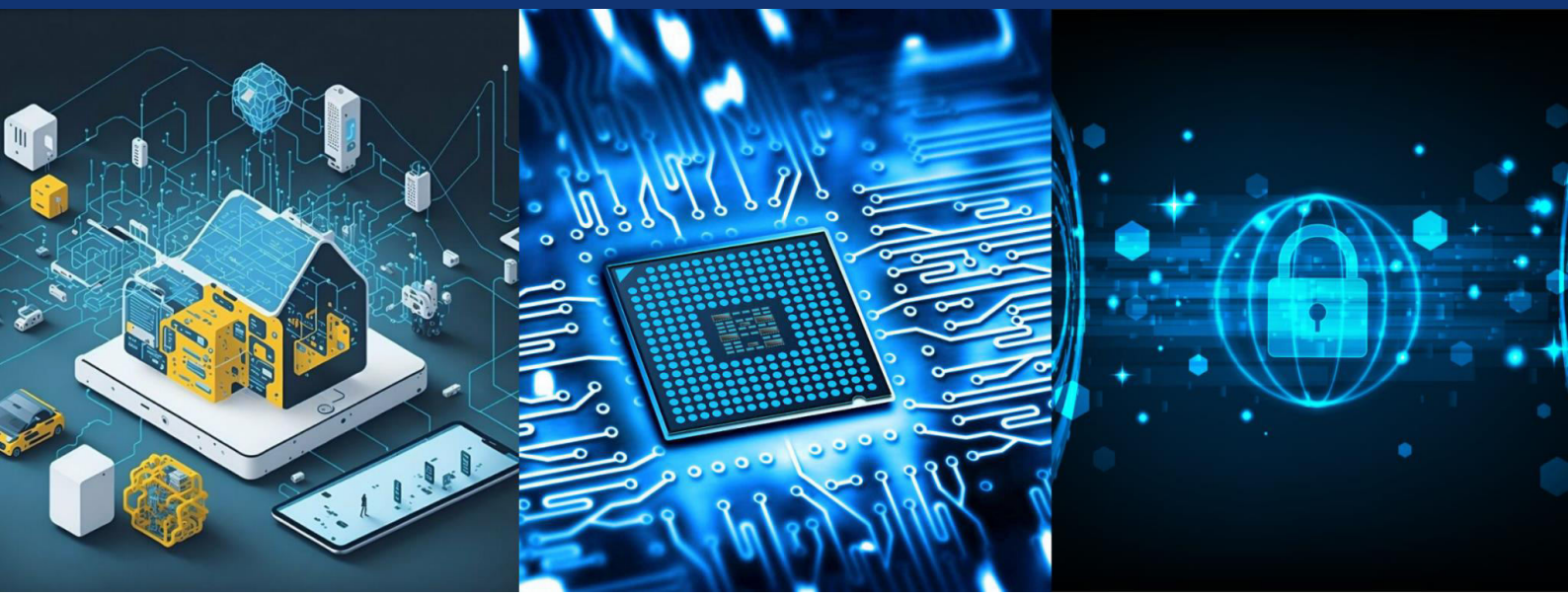
IJIRCCE

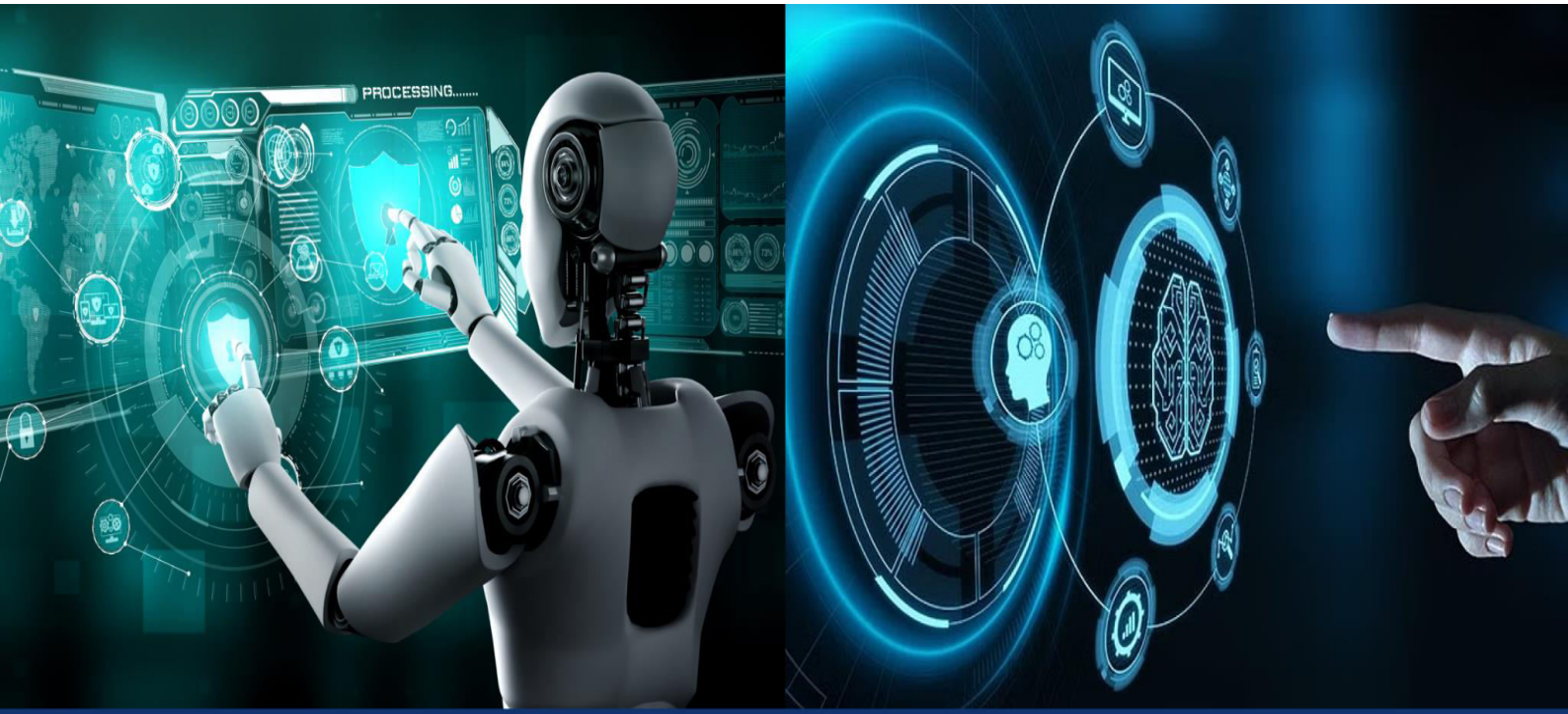
ISSN(O): 2320-9801

ISSN(P): 2320-9798



International Journal of Innovative Research in Computer and Communication Engineering

(A Monthly, Peer Reviewed, Refereed, Scholarly Indexed, Open Access Journal)



Impact Factor: 8.771

Volume 13, Issue 4, April 2025

© 2025 IJIRCCE | Volume 13, Issue 4, April 2025| DOI: 10.15680/IJIRCCE.2025.1304188

www.ijircce.com | e-ISSN: 2320-9801, p-ISSN: 2320-9798| Impact Factor: 8.771| ESTD Year: 2013|

International Journal of Innovative Research in Computer and Communication Engineering (IJIRCCE)

(A Monthly, Peer Reviewed, Refereed, Scholarly Indexed, Open Access Journal)

Design and Analysis of a Low-Power 5:2 Compressor based Approximate Multiplier with Reconfigurable Truncation

N.Nagaraju

Assistant Professor, Department of ECE, Sri Vasavi Institute of Engineering & Technology (Autonomous), Nandamuru, Pedana, A.P, India

B.Nandini, T.G.N.S.Sunitha, M.Mounika, M.Durga Rao

Department of ECE, Sri Vasavi Institute of Engineering & Technology (Autonomous), Nandamuru, Pedana, A.P, India

ABSTRACT: In modern digital systems, power-efficient and high-performance arithmetic circuits are essential for applications such as digital signal processing (DSP), image processing, and artificial intelligence (AI). Multipliers are fundamental components in such systems, and optimizing their design can significantly impact overall performance. This paper presents a novel low-power and high-accuracy 5:2 compressor based approximate multiplier with reconfigurable truncation to balance energy efficiency and computational precision. The proposed design reduces power consumption and area while maintaining acceptable accuracy levels. Simulation results demonstrate that our approach achieves substantial reductions in power and delay compared to conventional exact multipliers, making it highly suitable for error-tolerant applications.

KEYWORDS: Approximate Multiplier, Reconfigurable Truncation, Low Power VLSI Design, Digital Signal Processing (DSP).

I. INTRODUCTION

Approximate computing has emerged as a promising technique to enhance power and performance efficiency in error-tolerant applications. Conventional multipliers are power-intensive, making them less suitable for resource-constrained embedded and real-time systems. To address this challenge, we propose a **5:2 compressor-based approximate multiplier** that incorporates **reconfigurable truncation** to dynamically adjust accuracy and power trade-offs. This approach optimally reduces redundant computations while preserving the essential bits for high-accuracy results.

Our design is evaluated based on parameters such as **power consumption, delay, and accuracy**, demonstrating its efficiency for real-world applications. With the rapid advancement of digital systems, power-efficient and high-performance arithmetic units have become crucial for modern computing applications, particularly in areas such as digital signal processing, machine learning, and image processing. Multipliers, as fundamental components of these systems, significantly impact power consumption and computational speed. However, traditional multipliers demand substantial power and area, leading to challenges in designing energy-efficient circuits.

Approximate computing has emerged as a promising paradigm to address these challenges by leveraging the inherent error tolerance in many applications. By trading off a small amount of accuracy, approximate multipliers can achieve significant reductions in power consumption, delay, and silicon area. Among the various techniques, truncation is a widely used approximation method that discards less significant bits to minimize power and complexity. However, fixed truncation schemes lack flexibility, leading to suboptimal accuracy for varying application requirements.

This project explores the design and implementation of a low-power and high-accuracy approximate multiplier using reconfigurable truncation. The proposed design leverages transmission gate logic, known for its low-power

www.ijircce.com | e-ISSN: 2320-9801, p-ISSN: 2320-9798| Impact Factor: 8.771| ESTD Year: 2013|

International Journal of Innovative Research in Computer and Communication Engineering (IJIRCCE)

(A Monthly, Peer Reviewed, Refereed, Scholarly Indexed, Open Access Journal)

characteristics and high-speed operation, to achieve efficient multiplication. The reconfigurable truncation technique enables dynamic adjustment of accuracy and power consumption, making the multiplier adaptable to different application scenarios.

By employing transmission gate logic, the multiplier benefits from reduced power dissipation, lower leakage currents, and enhanced speed compared to conventional CMOS logic designs. The reconfigurable truncation mechanism further enhances the design's versatility, allowing a balanced trade-off between accuracy and energy efficiency.

This project aims to provide an innovative solution to meet the growing demand for power-efficient arithmetic units while maintaining high computational accuracy. The proposed approximate multiplier is expected to contribute to the development of energy-efficient digital systems, particularly for error-resilient applications Multipliers are among the most critical arithmetic functional units in many applications, such as digital signal processing (DSP), computer vision, multimedia processing, image recognition, and artificial intelligence. Those applications commonly need numerous multiplications that result in huge power consumption. The high-power consumption is a challenge for implementing those applications, especially on mobile devices. Therefore, many studies have proposed techniques to reduce the power consumption of multiplier circuits. One solution to reduce the power consumption of a multiplier is to approximate multiplication if the targeted applications allow error tolerance, or in other words, if they are related to human senses. Due to the human sensory limitations, such as limited viewing spectrum and hearing range, the accurate computing results are not necessary Approximate multipliers can be categorized into two types. The first type is to control the timing path of the multiplier, which can be achieved by using the dynamic voltage scaling. If a lower voltage is applied to a multiplier, the delay of the critical path will increase. Therefore, when the violation of the timing path happens, the errors occur, generating approximate results. The second type is to modify the functional behaviors of multipliers, which is to redesign the accurate multiplier circuits e.g., Wallace Tree Multiplier and Dadda Tree multiplier. Among the redesigning multipliers, most of the previous works proposed inaccurate m-n compressors that have m inputs and generate n outputs. These inaccurate com- pressors were used to compress the partial products within multiplication since the procedure of compressing partial products consumed most of the multiplier energy and caused long path delay.

Most of these previous approximate multipliers only pro- vided fixed output accuracy and fixed required power. How- ever, the ability to dynamically adjust accuracy and power consumption is useful for some applications, such as artificial intelligence whose requirement is changing over time. Note that in order to achieve an adjustable multiplier design, additional hardware cost is unavoidable

In this work, we propose a high accuracy 4-2 compressor, based on which, we further design a high accuracy approximate multiplier. In addition, we propose a dynamic input truncation technique to adjust the accuracy and required power. The contributions of the paper are summarized as follows:
We propose a high accuracy approximate 4-2 compressor that can be used to construct the proposed approximate multiplier.

We design a simple error compensation circuit to further reduce the error distance.
We propose a dynamic input truncation technique that can be used to adjust accuracy and power required for a multiplication. The proposed technique issuitable for CNNs as power consumption can be easily adjusted depending on the different requirements for each layer.

Based on the proposed 4-2 compressor, error compensation circuit and the dynamic input truncation technique, we propose a high-accuracy and reconfigurable approximate multiplier.

The design and analysis of a low-power 5:2 compressor-based approximate multiplier with reconfigurable truncation represents a sophisticated and efficient approach to digital multiplication, particularly suited for applications where power efficiency, speed, and area optimization are critical. This project integrates three major innovations—5:2 compressor logic, approximate computing, and reconfigurable truncation—into a single 8×8 multiplication architecture, enhancing performance while managing trade-offs in accuracy and hardware cost. The core idea stems from the need to optimize the traditional multiplication process by reducing the number of partial product rows and managing carry propagation efficiently, thus minimizing critical path delay and dynamic power consumption.

© 2025 IJIRCCE | Volume 13, Issue 4, April 2025| DOI: 10.15680/IJIRCCE.2025.1304188

www.ijircce.com | e-ISSN: 2320-9801, p-ISSN: 2320-9798| Impact Factor: 8.771| ESTD Year: 2013|

International Journal of Innovative Research in Computer and Communication Engineering (IJIRCCE)

(A Monthly, Peer Reviewed, Refereed, Scholarly Indexed, Open Access Journal)

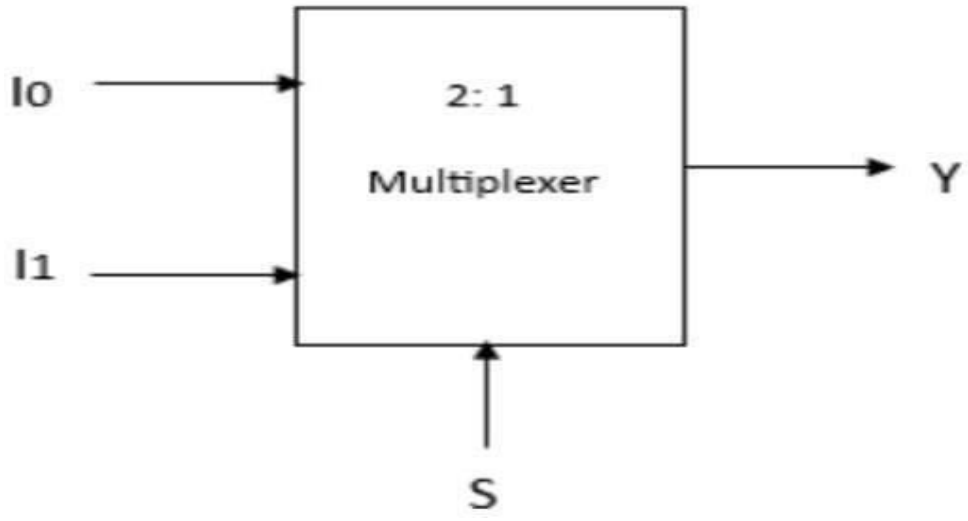
II. PROPOSEDSYSTEM

The design and analysis of a low-power 5:2 compressor-based approximate multiplier with reconfigurable truncation represents a sophisticated and efficient approach to digital multiplication, particularly suited for applications where power efficiency, speed, and area optimization are critical. This project integrates three major innovations—5:2 compressor logic, approximate computing, and reconfigurable truncation—into a single 8×8 multiplication architecture, enhancing performance while managing trade-offs in accuracy and hardware cost. The core idea stems from the need to optimize the traditional multiplication process by reducing the number of partial product rows and managing carry propagation efficiently, thus minimizing critical path delay and dynamic power consumption.

The use of a 2×1 multiplexer for dynamic precision adjustment in the proposed system allows the multiplication process to be highly flexible and energy-efficient. A 2×1 multiplexer is a simple digital switch that selects one of two inputs based on a control signal, effectively enabling the system to choose between two possible outcomes.

In the context of the Reconfigurable Truncation-Based Approximate Multiplier, this multiplexer is used to select between different levels of precision during multiplication. The multiplier works by truncating the least significant bits (LSBs) of the multiplication result to reduce both power consumption and circuit complexity. By dynamically adjusting the multiplexer's control signal, the system can either keep the full precision of the multiplication or discard some of the LSBs, depending on the application's error tolerance and performance requirements. This dynamic selection of precision allows the multiplier to operate with lower energy and faster performance when high precision is not needed, making the system highly adaptable and efficient.

As a result, the 2×1 multiplexer plays a crucial role in enabling adaptive precision control, allowing the multiplier to be optimized for energy-efficient computation in various applications such as image processing or machine learning.



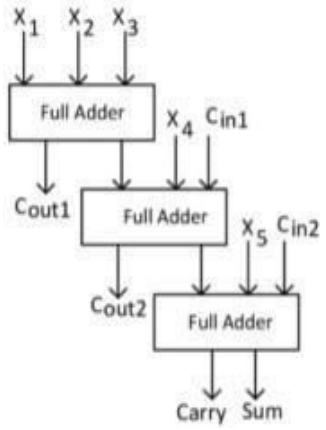
In an 8×8 multiplier, the product of two 8-bit operands results in up to 64 partial bits which must be summed. Traditionally, these are processed using full adders or Wallace/Dadda trees, but the proposed design leverages 5:2 compressors to perform multi-bit summation in fewer clock cycles. A 5:2 compressor takes five input bits and two carry- in bits and compresses them into three outputs (Sum, Carry, and Carry- Out), reducing the height of the partial product tree effectively. This leads to fewer intermediate stages, lower switching activity, and reduced propagation delay, which are crucial for high-speed multipliers.

© 2025 IJIRCCE | Volume 13, Issue 4, April 2025| DOI: 10.15680/IJIRCCE.2025.1304188

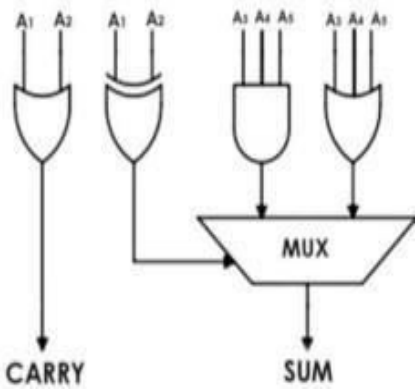
www.ijircce.com | e-ISSN: 2320-9801, p-ISSN: 2320-9798| Impact Factor: 8.771| ESTD Year: 2013|

International Journal of Innovative Research in Computer and Communication Engineering (IJIRCCE)

(A Monthly, Peer Reviewed, Refereed, Scholarly Indexed, Open Access Journal)



Accurate 5:2 compressor



Approximate 5:2 compressor

To further enhance power efficiency and reduce circuit complexity, the multiplier employs approximate computing principles. This involves strategically introducing controlled inaccuracies in less significant bit positions where errors have negligible impact on overall output quality. These approximations are applied in the partial product reduction stage, typically in the lower half of the product matrix. Approximate 5:2 compressors are designed by simplifying gate logic—removing or modifying carry propagation logic—thereby achieving lower gate count, area, and power at the cost of minimal and acceptable error margins.

The third innovation—reconfigurable truncation—adds versatility and dynamic control to the multiplier. Truncation involves omitting the least significant bits from computation, which further reduces power and hardware resource usage. Unlike static truncation, reconfigurable truncation allows the system to dynamically select how many bits to truncate based on performance or energy constraints. This is particularly beneficial in systems like adaptive signal processing, IoT, and machine learning accelerators where workload requirements can vary over time. The truncation module uses control signals to selectively disable sections of the partial product matrix and corresponding adders, offering runtime flexibility between accuracy and efficiency.

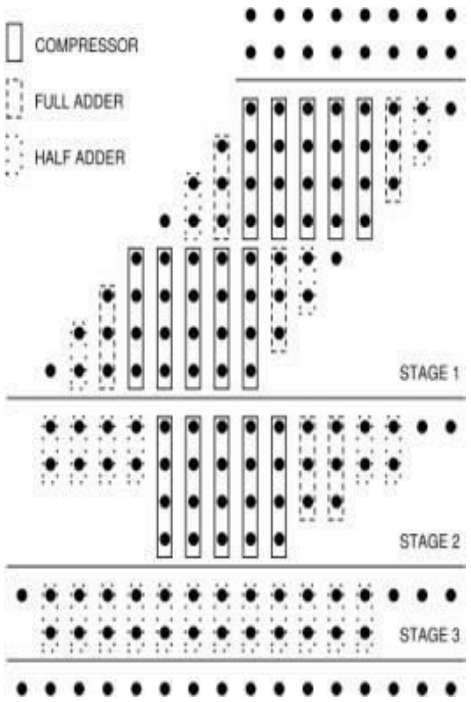
The Verilog HDL implementation of the design includes modules for exact and approximate 5:2 compressors, a control unit for reconfigurable truncation, and a top-level 8×8 multiplier module that integrates these components. Simulation and synthesis are performed using standard EDA tools, verifying functionality, delay, area, and power consumption. Comparative analysis against traditional 8×8 multipliers (such as Wallace or Dadda-based) confirms the superiority of the proposed design in terms of power-delay product (PDP), with substantial reductions in power and latency observed under typical operating conditions.

© 2025 IJIRCCE | Volume 13, Issue 4, April 2025| DOI: 10.15680/IJIRCCE.2025.1304188

www.ijircce.com | e-ISSN: 2320-9801, p-ISSN: 2320-9798| Impact Factor: 8.771| ESTD Year: 2013|

International Journal of Innovative Research in Computer and Communication Engineering (IJIRCCE)

(A Monthly, Peer Reviewed, Refereed, Scholarly Indexed, Open Access Journal)



Proposed 8*8 Approximate Multiplier

A	B	C	D	E	Cin1	Cin2	X (Total 1's)	C2	C1	S
0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1	0	0	1
1	1	0	0	0	0	0	2	0	1	0
1	1	1	0	0	0	0	3	0	1	1
1	1	1	1	0	0	0	4	1	0	0
1	1	1	1	1	0	0	5	1	0	1
1	1	1	1	1	1	0	6	1	1	0
1	1	1	1	1	1	1	7	1	1	1

Trurh Table for Approximate 5:2 Compressor

© 2025 IJIRCCE | Volume 13, Issue 4, April 2025| DOI: 10.15680/IJIRCCE.2025.1304188

www.ijircce.com | e-ISSN: 2320-9801, p-ISSN: 2320-9798| Impact Factor: 8.771| ESTD Year: 2013|

International Journal of Innovative Research in Computer and Communication Engineering (IJIRCCE)

(A Monthly, Peer Reviewed, Refereed, Scholarly Indexed, Open Access Journal)

III. EXPERIMENTAL RESULTS

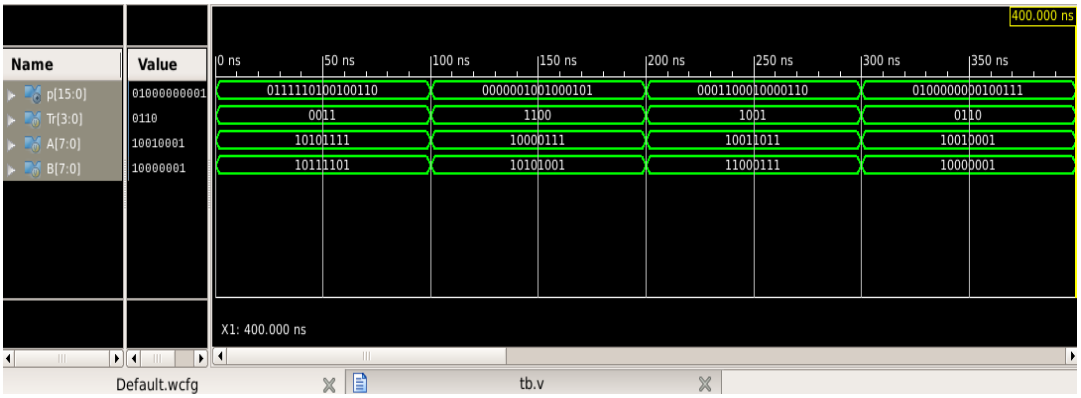


Fig.1.Simulation Result

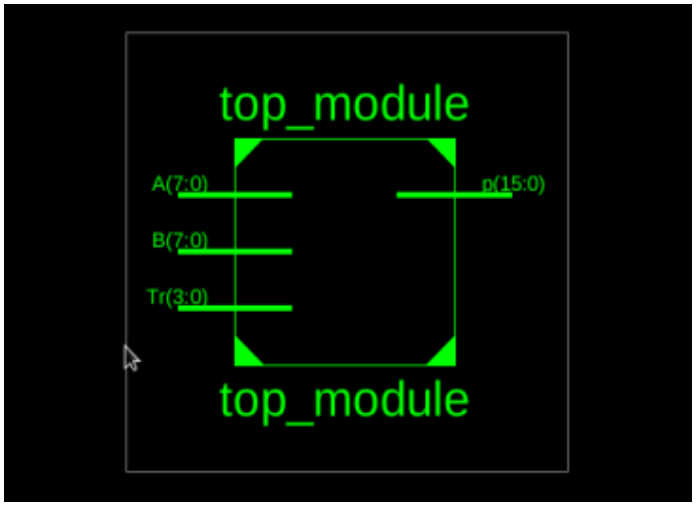


Fig.2.Block Diagram

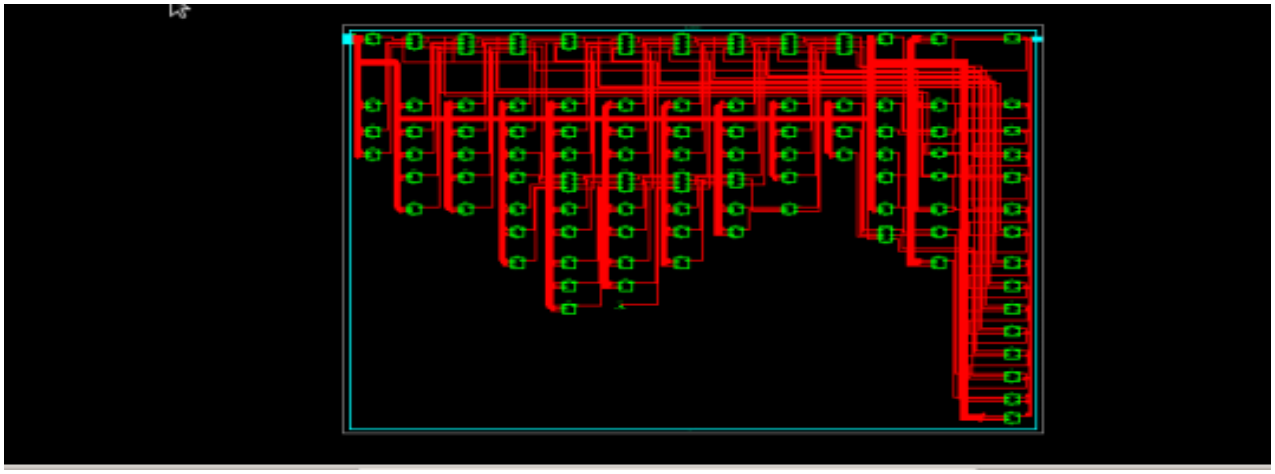


Fig.3.RTL Schematic

© 2025 IJIRCCE | Volume 13, Issue 4, April 2025| DOI: 10.15680/IJIRCCE.2025.1304188

www.ijircce.com | e-ISSN: 2320-9801, p-ISSN: 2320-9798| Impact Factor: 8.771| ESTD Year: 2013|

International Journal of Innovative Research in Computer and Communication Engineering (IJIRCCE)

(A Monthly, Peer Reviewed, Refereed, Scholarly Indexed, Open Access Journal)

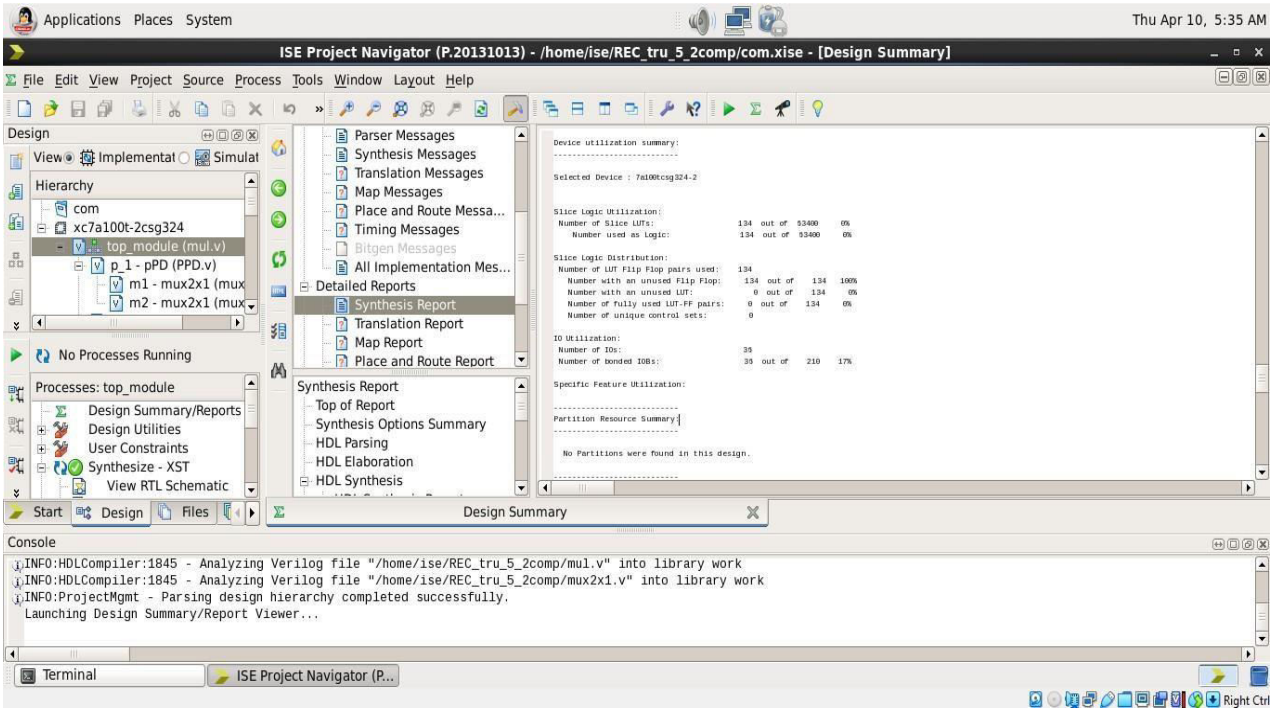


Fig.4.Device Utilization

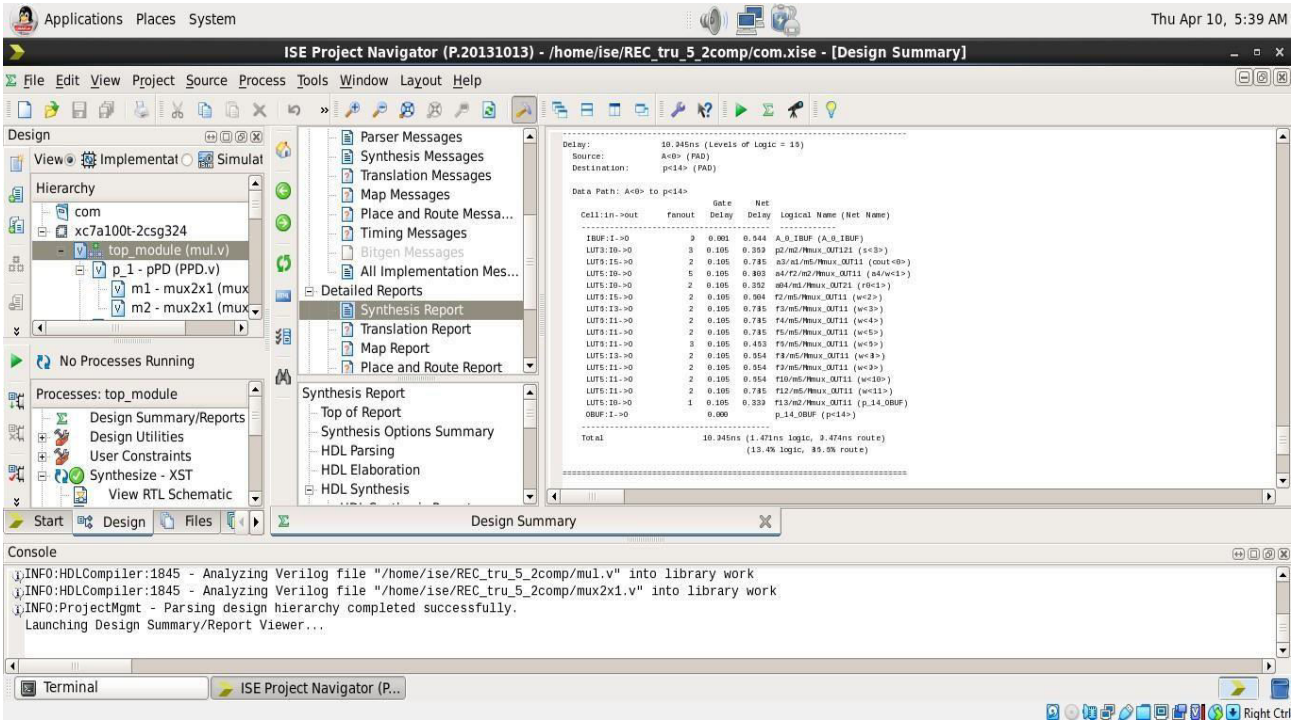


Fig.5.Delay Report

© 2025 IJIRCCE | Volume 13, Issue 4, April 2025| DOI: 10.15680/IJIRCCE.2025.1304188

www.ijircce.com | e-ISSN: 2320-9801, p-ISSN: 2320-9798| Impact Factor: 8.771| ESTD Year: 2013|

International Journal of Innovative Research in Computer and Communication Engineering (IJIRCCE)

(A Monthly, Peer Reviewed, Refereed, Scholarly Indexed, Open Access Journal)

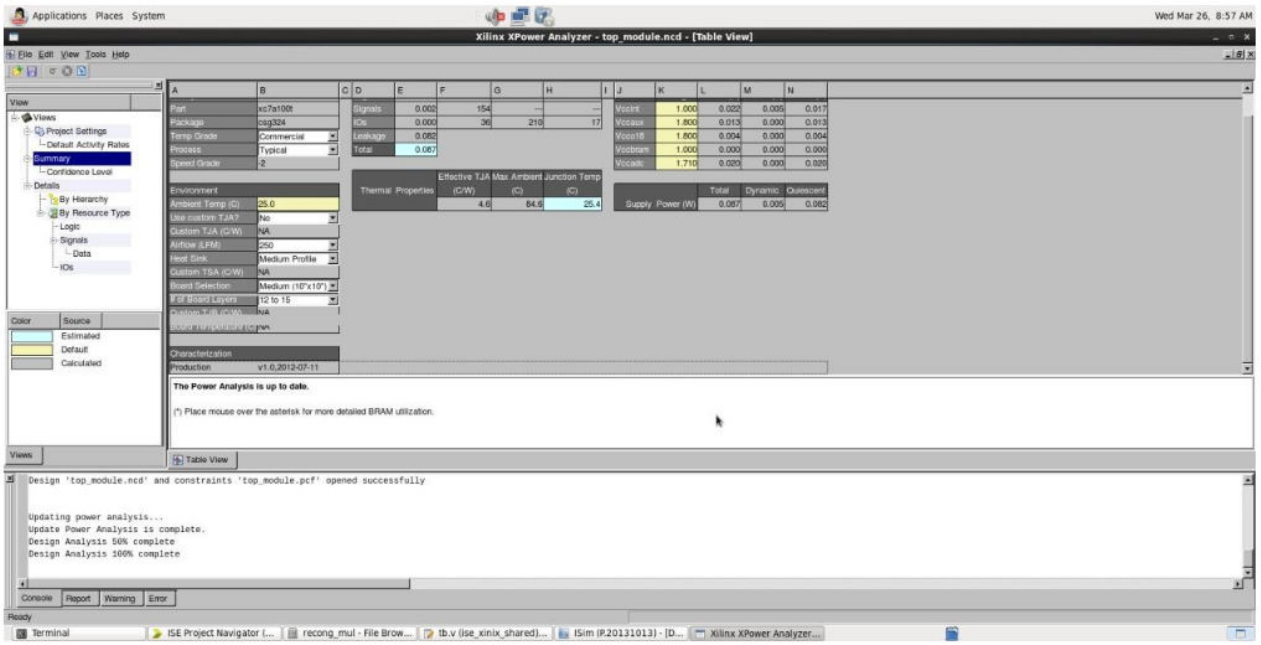


Fig.6.Power Report

IV. CONCLUSION

Introduces a 5:2 compressor-based approximate multiplier with reconfigurable truncation, demonstrating significant reductions in power and area while maintaining acceptable accuracy. The proposed design achieves high-speed computation and low-power consumption, making it an ideal candidate for error-tolerant applications. Simulation results validate the effectiveness of the approach, proving its advantages over traditional exact multipliers.

REFERENCES

1. FANG-YI GU, ING-CHAO LIN and JIA-WEI LIN, "A Low-Power and High-Accuracy Approximate Multiplier with Reconfigurable Truncation, " Published in IEEE Access ,May 2022 Digital object Identifier 10.1109/ACCESS.2022.3179112.
2. B. Moons and M. Verhelst, ''DVAS: Dynamic voltage accuracy scaling for increased energyefficiency in approximate computing,'' in Proc. IEEE/ACM Int. Symp. Low Power Electron. Design (ISLPED), Jul. 2015, pp. 237–242.
3. D. Mohapatra, V. K. Chippa, A. Raghunathan, and K. Roy, ''Design of voltage-scalable metafunctions for approximate computing,'' in Proc. Design, Autom. Test Eur., Mar. 2011, pp. 1–6.
4. K. Yin Kyaw, W. Ling Goh, and K. Seng Yeo, ''Low-power high-speed multiplier for errortolerant application,'' in Proc. IEEE Int. Conf. Electron Devices Solid-State Circuits (EDSSC), Dec. 2010, pp. 1–4.
5. M. de la Guia Solaz, W. Han, and R. Conway, ''A flexible low power DSP with a programmable truncated multiplier,'' IEEE Trans. Circuits Syst., vol. 59, no. 11, pp. 2555–2568, Nov. 2012.
6. R. Zendegani, M. Kamal, M. Bahadori, A. Afzali-Kusha, and M. Pedram, ''RoBa multiplier: A rounding-based approximate multiplier for high- speed yet energy-efficient digital signal processing,'' IEEE Trans. Very Large-Scale Integer. (VLSI) Syst., vol. 25, no. 2, pp. 393–401, Feb. 2017.
7. C. S. Wallace, ''A suggestion for a fast multiplier,'' IEEE Trans. Electron. Comput., vol. EC13, no. 1, pp. 14– 17, Feb. 1964.
8. A. Weinberger, '4:2 carry-save adder module,'' IBM Tech. Discl. Bull., vol. 23, no. 8, pp. 3811–3814, 1981.
9. A. Momeni, J. Han, P. Montuschi, and F. Lombardi, ''Design and analysis of approximate compressors for multiplication,'' IEEE Trans. Compute., vol. 64, no. 4, pp. 984–994, Apr. 2015.

www.ijircce.com | e-ISSN: 2320-9801, p-ISSN: 2320-9798| Impact Factor: 8.771| ESTD Year: 2013|

International Journal of Innovative Research in Computer and Communication Engineering (IJIRCCE)

(A Monthly, Peer Reviewed, Refereed, Scholarly Indexed, Open Access Journal)

10. Z. Yang, J. Han, and F. Lombardi, ''Approximate compressors for error- resilient multiplier design,'' in Proc. IEEE Int. Symp. Defect Fault Tolerance VLSI Nanotechnology. Syst. (DFTS), Oct. 2015, pp. 183–186.
11. 11] C.-H. Lin and I.-C. Lin, ''High accuracy approximate multiplier with error correction,'' in Proc. IEEE 31st Int. Conf. Comput. Design (ICCD), Oct. 2013, pp. 33–38.
12. P. J. Edavoor, S. Raveendran, and A. D. Rahulkar, ''Approximate multiplier design using novel dual-stage 4:2 compressors,'' IEEE Access, vol. 8,pp. 48337–48351, 2020.
13. F. Sabetzadeh, M. H. Moaiyeri, and M. Ahmadinejad, ''A majority-based imprecise multiplier for ultra- efficient approximate image multiplication,'' IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 66, no. 11, pp. 4200– 4208, Nov. 2019.
14. A. G. M. Strollo, E. Napoli, D. De Caro, N. Petra, and G. D. Meo, ''Comparison and extension of approximate 4–2 compressors for low- power approximate multipliers,'' IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 67, no. 9, pp. 3021–3034, Sep. 2020.
15. H. Xiao, H. Xu, X. Chen, Y. Wang, and Y. Han, ''Fast and high-accuracy approximate MAC unit design for CNNcomputing,'' IEEE Embedded Syst. Lett., early access, Dec. 21, 2021, Doi: 10.1109/LES.2021.3137335.
16. O. Akbari, M. Kamal, A. Afzali-Kusha, and M. Pedram, ''Dual-quality 4:2 compressors for utilizing in dynamic accuracy configurable multipli-ere,'' IEEE Trans. Very Large-Scale Integer. (VLSI) Syst., vol. 25, no. 4,pp. 1352–1361, Apr. 2017.
17. T. Yang, T. Ukezono, and T. Sato, ''A low-power high-speed accuracy- controllable approximate multiplier design,'' in Proc. 23rd Asia South Pacific Design Autom. Conf. (ASP-DAC), Jan. 2018, pp. 605–610.
18. I. Hammad, L. Li, K. El-Sankary, and W. M. Snelgrove, ''CNN inference using a preprocessing precision controller and approximate multipliers with various precisions,'' IEEE Access, vol. 9, pp. 7220–7232, 2021.
19. C. Guo, L. Zhang, X. Zhou, W. Qian, and C. Zhuo, ''A reconfigurable approximate multiplier for quantized CNN applications,'' in Proc. 25th Asia South Pacific Design Autom. Conf. (ASP-DAC), Jan. 2020,pp. 235–240.
20. B. Jacob, S. Kligys, B. Chen, M. Zhu, M. Tang, A. Howard, H. Adam, and D. Kalenichenko, ''Quantization and training of neural networks for efficient integer-arithmetic-only inference,'' in Proc. IEEE/CVF Conf. Comput. Vis. Pattern Recognit., Jun. 2018, pp. 2704–2713.
21. P.-Y. Chen, F.-Y. Gu, Y.-H. Huang, and I.-C. Lin, ''WRAP: Weight RemApping and processing in RRAM- based neural network accelerators considering thermal effect,'' in Proc. Design, Autom. Test Eur. Conf. Exhib. (DATE), Mar. 2022, pp. 1245–1250.

INTERNATIONAL STANDARD SERIAL NUMBER INDIA

INNO SPACE SJIF Scientific Journal Impact Factor

doi crossref

निस्केयर NISCAIR

INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH

IN COMPUTER & COMMUNICATION ENGINEERING

9940 572 462 6381 907 438 ijircce@gmail.com

www.ijircce.com

Scan to save the contact details