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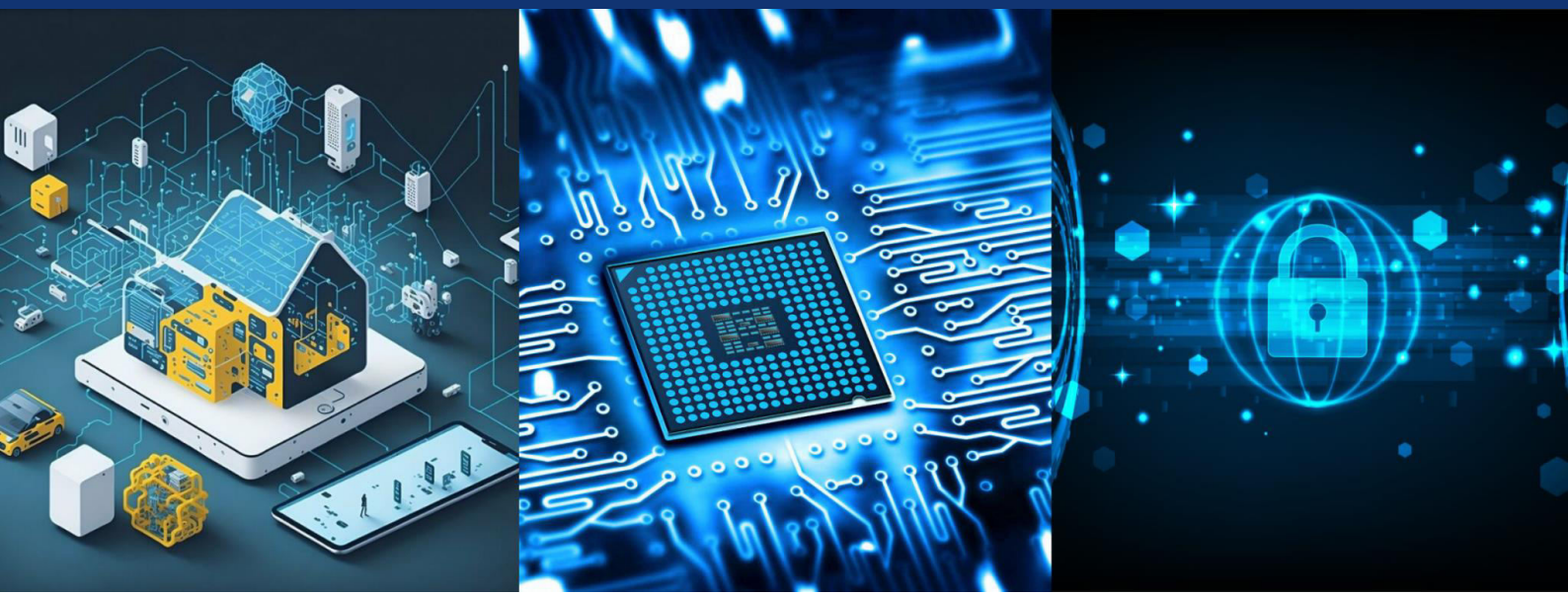

International Journal of Innovative Research in Computer and Communication Engineering

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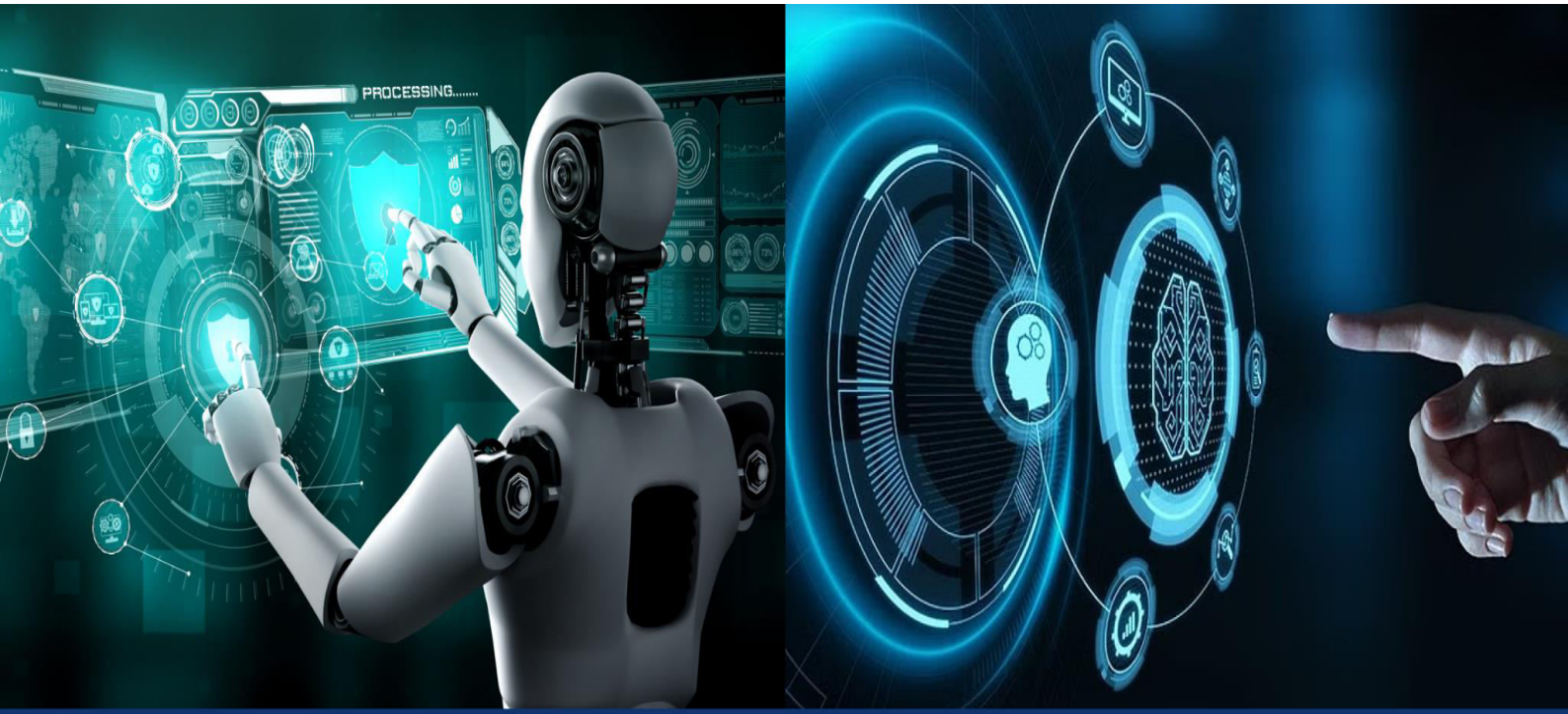

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International Journal of Innovative Research in Computer and Communication Engineering (IJIRCCE)

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Design an Area Efficient Kogge Stone Adder Using Pass Transistor Logic of 22nm

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ABSTRACT: The design of an area-efficient Kogge-Stone Adder (KSA) using pass transistor logic (PTL) in 22nmtechnology focuses on optimizing the performance, power, and area of high-speed arithmetic units used in modern computing architectures. The Kogge-Stone Adder is a widely used parallel prefix adder known for its fast carry propagation, making it ideal for applications requiring high-speed arithmetic computations, such as digital signal processing (DSP), microprocessors, and cryptographic systems. However, traditional KSA designs suffer from increased area and power consumption due to their complex interconnection and large transistor count. To overcome these challenges, pass transistor logic (PTL) is integrated into the design to significantly reduce transistor count and improve area efficiency

KEYWORDS Pass Transistor Logic, Kogge Stone Adder, Area consumption, , Parallel Prefix Adder,22nm Technology, Tanner EDA.

I. INTRODUCTION

The Kogge-Stone Adder (KSA) is a fast and efficient type of binary adder used in digital circuits, especially in modern processors where speed is very important. It is designed to add two binary numbers by calculating all the necessary carry values in parallel, instead of waiting for each carry to move from one bit to the next. In traditional adders like the ripple carry adder, each bit has to wait for the carry from the previous bit, which takes time and slows down the addition process. The Kogge-Stone adder avoids this delay by using a special tree structure made of logic gates that can compute all carry signals at the same time. This is known as a parallel prefix computation PASS Transistor Logic :Pass Transistor Logic involves nMOS or pMOS transistors to transfer the charge from one node of a circuit to another node under the control of MOS gate voltage.In traditional CMOS logic, each logic function requires a complementary pair of transistors (one PMOS and one NMOS). In contrast, PTL uses a single transistor to implement logic functions, reducing the transistor count.

II.PROPOSEDSYSTEM

Kogge Stone Adder using Pass Transistor Logic uses 22nm technology transistors.
In 22nm technology, the transistors have a much smaller channel length, leading to lower area consumption, better speed, and improved efficiency.
The system uses fewer transistors and benefits from the compact and high-speed features of 22nm CMOS design, which helps reduce overall circuit complexity.
Power usage: significantly reduced due to improved tec
Results for the PTL KSA (in 22nm):
Power usage: lower than in the 120nm version due to better transistor performance
Area: more compact layout compared to 120nm design
Delay :Delay will be reduced

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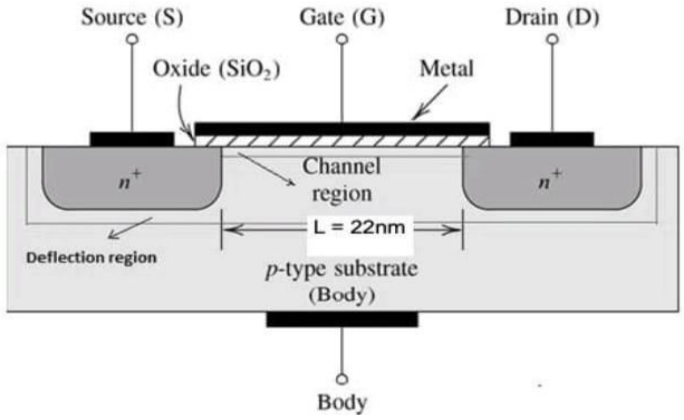

This study successfully shows that a 4-bit Kogge Stone Adder can be made smaller, faster, and more power-efficient by using Pass Transistor Logic combined with 22nm technology. With a reduced number of transistors, lower power consumption, and a smaller layout area, the new design is perfect for VLSI and DSP systems, where saving space is just as important as being fast.

III. EXPERIMENTAL RESULTS

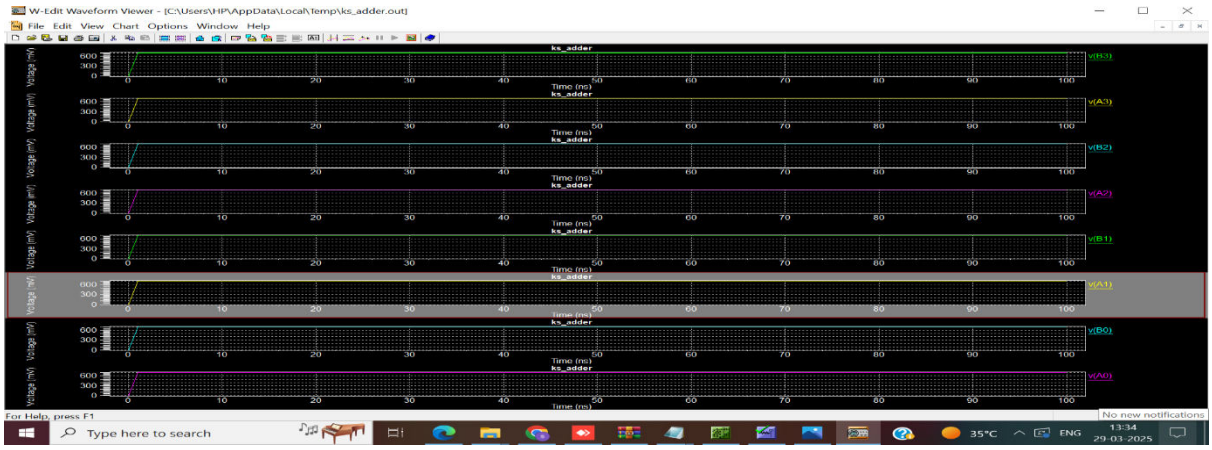

Fig.1.Inputs Wave forms of Proposed system

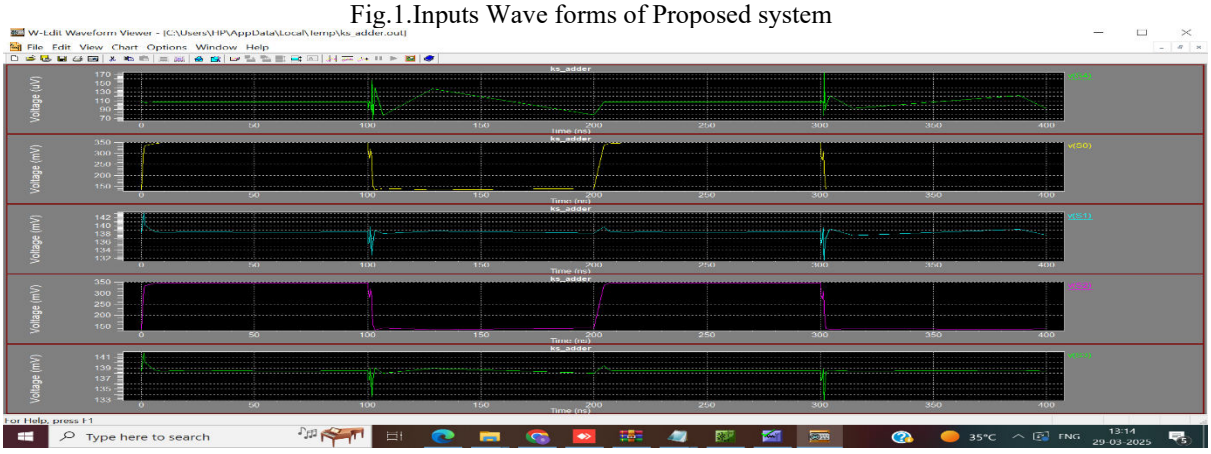

Fig:2: Output Wave forms of Proposed System

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Fig 3:Delay for proposed system

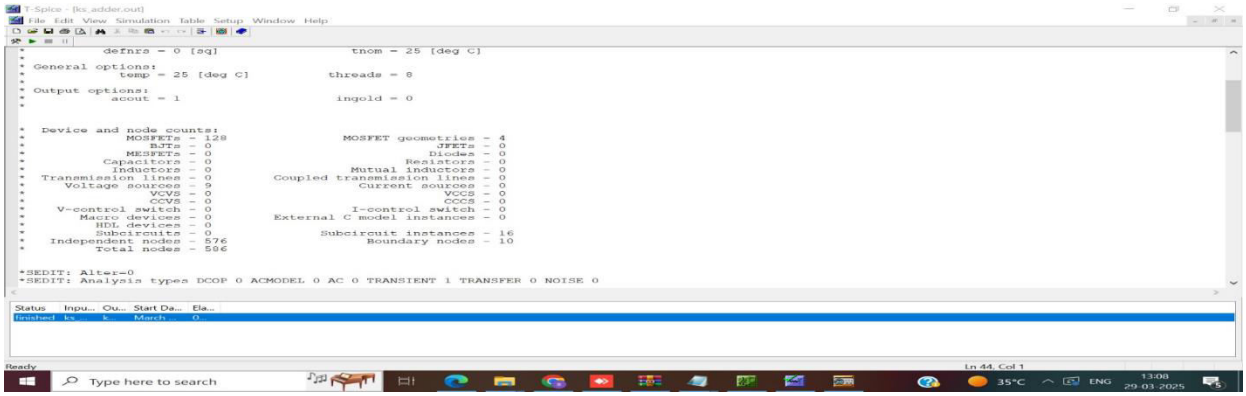

Fig 4:Transistor count in proposed system

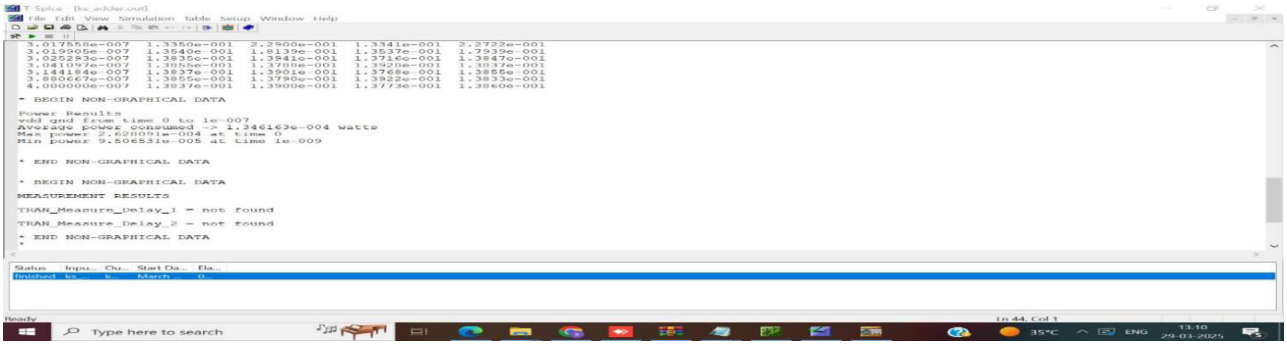

Fig 5: power consumption in proposed system

IV. CONCLUSION

In this project, a 4-bit Kogge-Stone Adder (KSA) was successfully designed and implemented using pass transistor logic in 22nm CMOS technology with the help of Tanner EDA tools. The main goal was to create a compact, high-speed adder by taking advantage of the efficient Kogge-Stone architecture and the reduced transistor count of pass transistor logic. The Kogge-Stone Adder is known for its fast carry generation and low delay, which makes it ideal for high-performance systems. By using pass transistor logic instead of traditional CMOS logic, the design used fewer transistors, which helped reduce the overall chip area. Simulations confirmed that the adder worked correctly for all input combinations and showed improved speed and lower power consumption. The physical layout in the 22nm technology node also showed efficient use of space, meeting the project's area-saving goals.

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In summary, this project shows that combining the Kogge-Stone architecture with pass transistor logic in advanced technology can be a great choice for fast and compact arithmetic circuits. Future work can expand this approach to larger adders and further explore the balance between power, speed, and area in more complex systems

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