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Power Analysis of 6T, 7T&8T SRAM Cells Using Tanner Tool at 45nm Technology

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ABSTRACT: The semiconductor industries have brought greater demand for low power consumption design for integrated circuits. The Static Random Access Memory (SRAM) has become one of the major components due to the large storage density and low power consumption. This paper implements different SRAM cell topologies such as 6T, 7T&8T. And its main objective is to evaluate its performance on the basis of static power, delay, area and frequency of SRAM cell in 45nm technology using TANNER TOOL.

KEYWORDS: SRAM, Dynamic Power, Static Power, Leakage Power, 45nm Technology.

I.INTRODUCTION

In many digital systems, semiconductor memory arrays are capable of storing a large amount of data. The number of transistors are used for the storage purpose is larger than the transistors use in logic operation and other purpose. The increasing demand of large storage capacity has driven the fabrication technology and compact size. The data storage capacity of semiconductor memory array approximately doubles in every two years. The area efficiency of the memory array is the number of storage bits per unit area is a key design factor which determines the total storage capacity.

The important factor is required time to store and retrieve data in a memory array. SRAM is mostly used in cache memory in microprocessors, memory in devices due to high speed and high power consumption. SRAM is a type of semiconductor memory which stores each bit of data. The power consumption of SRAM varies widely depending on frequency& Area. It is accessed in some times and it can used as much power as SRAM, it used at high frequencies, Static RAM used at a slower pace, such as in applications with moderately clocked Microprocessors, draws very little power and can have a nearly negligible power consumption when sitting idle in the region of a few micro-watts. Several techniques have been proposed to manage power consumption of SRAM-based memory Topologies.

II.LITERATURE SURVEY

The Static Random Access Memory is a type of memory that uses Bi-stable Latching Circuitry (flip flop) to store bit either 0(0r)1 .The SRAM exhibits data but it still volatile in the data is eventually lost the memory is not powered.The SRAM memory cell is 45nanometer technology node, high k+ metal Gate transistors have been introduced for first time in 45nm technology is used to roadmap for semiconductors. The High k+ dielectric contains a chipmakers have initially about introducing new high k+ materials into gate Stack, for a purpose of reducing leakage current density.

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Mrs.Sharmila Nath [1] characterised the performance which has brought greater demand for low power consumption design for Integrated circuits(IC).This paper represents different SRAM topologies such as 6T,7T&8T in 45nm technology and the main objective is to evaluate its performance on the basis of power, delay and area.
D.C, Arandilla, Anastacia B. Alvarez[2] characterised the performance of SRAM has been widely used in recent days due to its high performance in VLSI design techniques which operates in the range of nano range in the SRAM Cell the scaling of transistor will increase the stability of the cell at the time of read and write operations. There are several SRAM Cell has been designed which operates at the low voltage with less delay.Hence the construction of memories using SRAM Cell which is optimized in terms of area, power and delay.

Aminul Islam and Mohd Hassan[3] gives the ultra voltage operation of different SRAM cell. By lowering the supply voltage,the ultra voltage operation is performed.In this 6T SRAM topologies are evaluated for achieving low voltage operation. This Result are evaluated at 45nm technology,which clearly give the effectiveness of proposed bit cell for successive ultra low voltage operation.

Prajna Mishra, Eugene John and Wei-Ming Lin[4], this circuit contains a series connected transistor which turn down the leakage current because of this,cell achieves low power consumption.This 8T SRAM cell is compare with low power SRAM cell on 45nm technology, it gives the power reduced by 45.94% (0.4v) and 31.08% (0.3v) respectively.
we have designed different types of SRAM Cells And compares the performance of SRAM Cell Topologies 6T, 7T&8T SRAM Cell implementations interms of Leakage power, Static power, Dynamic power, delay& Area.

III. SRAM CELL

SRAM is a static random access memory that retains the data bits in its memory as long as power is supplied. SRAM is a type of semiconductor memory that uses Bi-stable latching circuitry to store each bit either 0 or 1. SRAM can give access time as low as 10nano seconds through it is more expensive. The usage of SRAM cell is continuously increasing in system on chip design. SRAM is very important because the cell area contributes significantly for silicon area.

45nanometer technology node, high-k+ metal Gate transistors have been introduced for first time in a high-k+ gate dielectric enabled 0.7 x reductions Tox. if The reducing gate leakage 1000x for PMOS and 25x for NMOS eliminating poly silicon gate depletion& providing compatibility with high-k+ dielectric in addition to high-k+ metal gate the 45nm gate length CMOS transistor have been integrated with 3rd generation of strained silicon for highest drive current for both NMOS.45nm technology is used to roadmap for semiconductors.It should refer for average half pitch of memory cell manufactured at around the 2007-2008 time frame.

The simulation has been done in tanner tool version 13.0.The performance analysis of SRAM cell has been evaluated in terms of power, delay and area.The Power,Area&Delay values are calculated based on netlist.

The Static power, Dynamic Power, Leakage Power delay, area and frequency for 6T,7T&8TSRAM cell are compared. The simulation is carried out using TANNER TOOL . Fig 1,3&5 shows 6T,7T&8T SRAM Cells respectively. Where as Fig 2,4&6 shows transient response of 6T,7T&8T SRAM Cells respectively.

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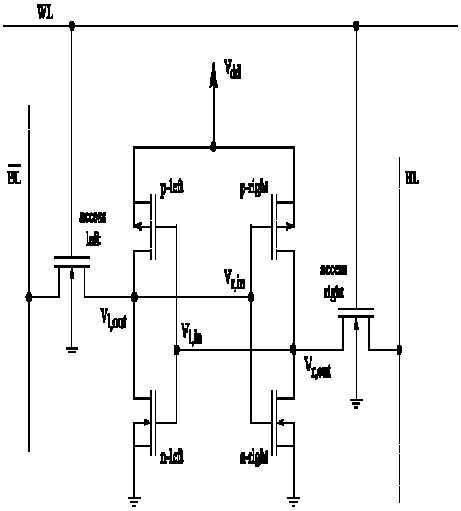

Fig.1Six Transistor (6T) SRAM Cell

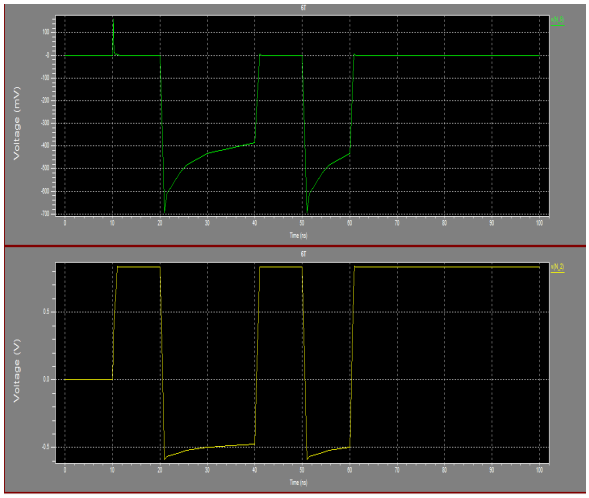

Fig:2 Transient Response of Six Transistor(6T)SRAM Cell

The Fig.1 shows the 6T SRAM bit cell which are connected to the same bit line at the time of write cycle. Because at the one set of a write cycle (when signal is activated), all the bit cells (or cross-coupled inverters) those sharing the same improving the write-ability of an accessed bit cell. While this bit cell topology takes more than 42% of area overhead as compared to standard 6T bit cell and to operate below 720mV but it manages to operate at sub-200mV.

The Structure of 6T SRAM consists of Six Transistors with the basic structure of the cell similar to the SRAM Cell. The Read signal W is pulsed to bit line(RBL) is used for reading data from the cell.

The Fig.2 shows of transient response the write operation, the Write signal W is pulsed to Vdd. And the input is applied to WL. While the read signal R is maintained at ground level. The access Transistors are accessed through the Write-line(W) and data is written in to cell. To start the Read operation the RBL is pre charged to vdd. The written data can be read from the cell by pre charging both RBL and Read line to the high level and maintaining Write line to Zero level. The storage nodes are completely isolated from the bit line during the read operation.

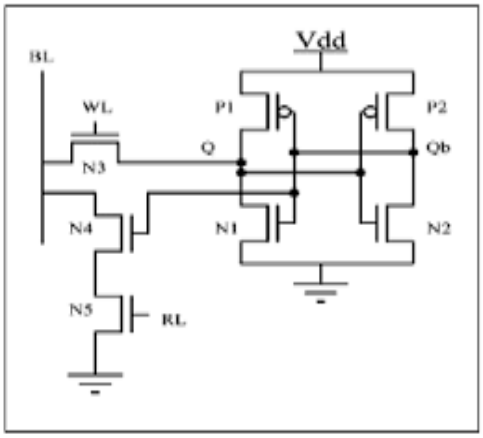

Fig.3.Seven Transistor (7T) SRAM Cell

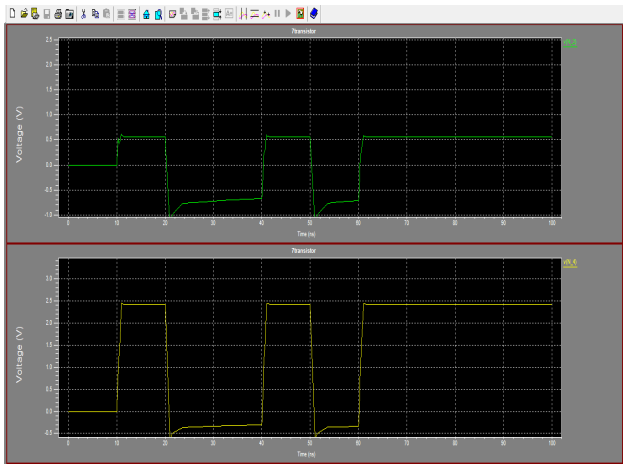

Fig. 4 Transient Response of (7T) SRAM Cell

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The Fig.3 shows the Structure of 7T SRAM consists of Seven Transistors with the basic structure of the cell similar to the conventional 6T SRAM Cell. The Read signal W is pulsed to bit line(RBL) is used for reading data from the cell.

The Fig.4 shows the transient response of write operation, the Write signal W is pulsed to Vdd. And the input is applied to WL.While the read signal R is maintained at ground level. The access Transistors are accessed through the Write-line(W) and data is written in to cell. To start the Read operation the RBL is pre charged to vdd. The written data can be read from the cell by pre charging both RBL and Read line to the high level and maintaining Write line to Zero level.The storage nodes are completely isolated from the bit line during the read operation.

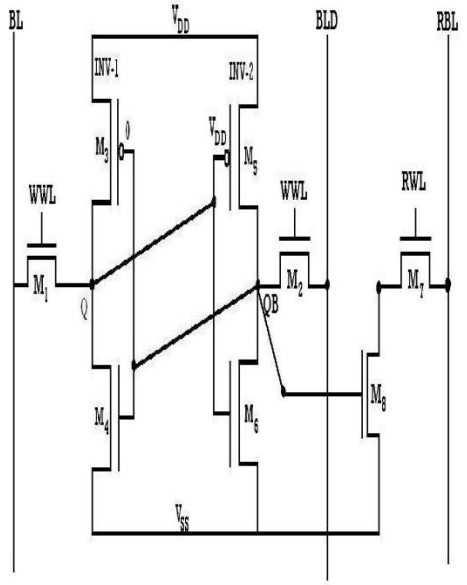

Fig.5 Eight Transistor (8T) SRAM Cell

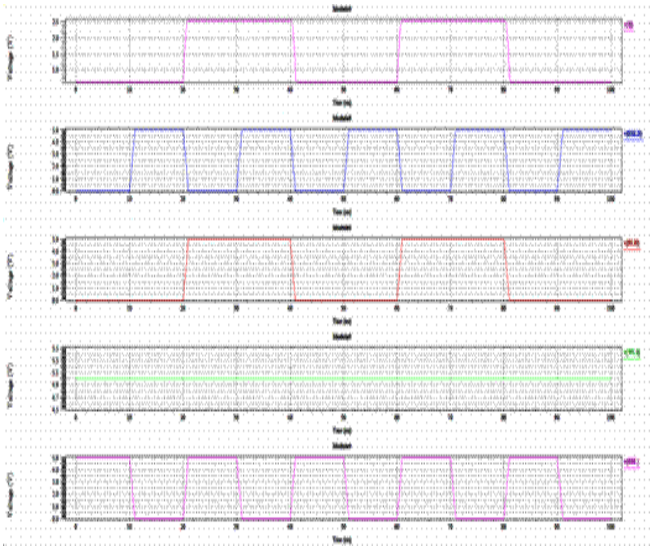

Fig.6 Transient Response of (8T) SRAM Cell

The fig.5 shows the Structure of 8T SRAM consists of Eight Transistors with the basic structure of the cell similar to the conventional 6T SRAM Cell. The Read signal W is pulsed to bit line (RBL) is used for reading data from the cell.

The Fig.6 shows the transient response of write operation, the Write signal W is pulsed to Vdd. And the input is applied to WL. While the read signal R is maintained at ground level. The access Transistors are accessed through the Write-line(W) and data is written in to cell. To start the Read operation the RBL is pre charged to vdd. The written data can be read from the cell by pre charging both RBL and Read line to the high level and maintaining Write line to Zero level.The storage nodes are completely isolated from the bit line during the read operation.

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IV. SIMULATION RESULTS

TABLE-1 Comparison of different SRAM Cell Topologies:

S.NO.	Parameter Name	6T	7T	8T
1	No.of cells/transistors	Six	Seven	Eight
2	Power	3.2 µw	4 µw	3.6 µw
3	Time	0.93 Sec	1.81 Sec	1.86 Sec
4	Frequency	1.80 Hz	1.75 Hz	0.53 Hz
5	Delay	0.01 ns	0.03 Ns	0.03 ns
6	Area	9 nm^2	21 nm^2	20 nm^2

V. CONCLUSION

This work deals with comparison of Power ,delay, area and frequency for 6T,7T&8T SRAM cells. The simulation is carried out using TANNER TOOL. The 6T,7T &8T SRAM cells have power consumption of 3.2 µw,4 µw&3.6 µw respectively. Where as delay is observed to be 0.01nsec,0.03nsec,0.03nsec respectively. From these simulation results it is observed that 6T SRAM Cell performs better when compared to other topologies in terms of speed.

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