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### **Optimization of PCB and VLSI Circuit Designing using Hybrid AI for Consumer Electronics Product**

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**ABSTRACT:** Placement and routing are two important issues regarding physical integration in integration. However, it cannot be synchronized between the two problems, and consider overload and vertebral length. Therefore, it is desirable to design efficient, that employs complex routing limits to shift cells and redesign the net, taking into account cell movement and complex routing limits. This paper uses a Routing which plays a very important role in the design of printed circuit boards (PCBs). The router has a big problem for selecting the shortest path results shows that to improve this and optimize the wirelength. The proposed technique reduces the overlap between the routing. This is used in the Optimization of PCB and VLSI Circuit Designing using Hybrid AI for Consumer Electronics Product.

KEYWORDS: Global routing, Printed circuit board, VLSI Circuits, MCTS

#### I. INTRODUCTION

Circuit design plays an important role in all household appliance products. Printed circuit boards (PCBs) and VLSI circuits (very large scale resolutions) require optimisation of electronic components and wire routing to connect components. Experts are now being carried out manually, and the cost of HR and time has increased dramatically. Such heuristic circuit structures are not optimized and have errors. For this reason, automated circular algorithms are important. However, it is a difficult NP problem, so it is difficult to get the best solution with circuit cost and weight as well as end of performance. Many techniques have been proposed to achieve routing optimization. In many technologies, some artificial intelligence (AI) have been used to improve overall performance and reduce design time. Therefore, routing problems are explained in PCB and VLSI, and the proposed techniques have been introduced to solve these routing problems. Therefore, you need a routing algorithm that finds a good enough solution.

First, apply 3D rabin-through routing with routing height limits based on wait queues. An estimate is then presented in the motion round of several cells. At each step of cell movement, the network routing limitations are taken into account. Finally, edge adjustment techniques are used to further improve the twisted wire. The algorithm reaches the optimal routing wire wire and conflict period without maximum cell migration limits. In recent years, extensive research has been conducted through the pen densities are high and physical limitations are clear. In addition, deeper universities have been proposed to generate areas recommended for routing algorithms.

The energy development of electronic information technology. The level of integration of components increasing, the number of pens increases, and the connections between components are becoming increasingly complicated. As a result, one of the challenging tasks of PCB design is the routing task. In industrial applications, considerable trust in manual PCB routing by engineers leads to significant time and HR resource consumption. Therefore, there is an urgent need for intelligent auto-routing algorithms that can be used in practical use in modern large scale electronic circuit designs to improve the design efficiency of electronic design automation (EDA). This directional study is divided into two main parts: surface routing and escape trout. The process of routing the pen within a component of a component is



called an escape process, and the process of routing between two components is called surface routing. However, the actual PCB structure usually consists of a number of components, such as passive devices, capacitor decoupling, and hole pinouts that are not components in the BGA package. These non-BGA pack components are usually irregularly distributed in PCB designs, leading to uneven distribution of traffic congestion, making routing tasks more difficult. Therefore, to tackle such problems, we need to develop a PCB routing algorithm.

#### **II. RELATED WORK**

As process technology drops further, the request for automatic extremely important market time to increase designs. The design flow of digital circuits was thoroughly supported by sophisticated design automation tools. However, analog circuits are more sensitive than digital circuits and layout effects of progressive technology nodes, so analog design and layout are performed manually in the industry. Therefore, analog designs are still based on the designer's expert knowledge to mitigate the effects of process variation on circuit performance. However, iterative improvements in manual designs can significantly increase the design cycle.

To increase productivity, you need the right automation tools. Due to a significant loss of designers are often unsatisfied with similar layouts generated by analog tools needs improvements. During the placement stage, the most important limitations are met with symmetry, proximity, and common center of gravity [3] [5]. This method deals with sewer for the PTL at the specified additional length. This is packed into a compact area based on simulated glow. Efficiently search for solutions using path generation methods from sequences of symbols. The tool allows you to generate a draft flow of HDL descriptions for layout generation. The Addier layout designed by the tool is displayed as experimental results. [4], [6], [7] have additional limitations during deployment to facilitate later routing tasks. It also provides a methodological approach for the strategic placement of trenches to protect against unwanted river traps. This section explains the implementation of PTL connections (passive transmission lines) and the physical arrangement of hybrid circuits.

In Progressive during the routing stage, analog circuits of analog circuits often correspond to the parasitic effects of several sensitive structures [1] [2]. Traffic dynamics have recently been adapted to the parasitic effects of analog circuits [10]. A significant improvement is an efficient routing (ER) strategy. In some circuits that require large current to drive other circuits, extension of wire width is an important methodology to reduce electrical drive problems [4].

Analog and Radio Frequency (A/RF)-IC Design Automation (IC) routing techniques have been proposed in the literature for over 30 years. In these, broad statements of geometric limitations are already treated as alternatives to routing quality, but performance-related criteria are also increasingly included. As A/RF designs have been transformed into progressive nodes of integrated technology, increasing design rules/limitations, wire resistance, traffic congestion, and inter-coupling growth are constantly a problem with existing automated routing techniques and put pressure on improving them. Fortunately, recent developments on modern workstations have enabled highly developed routing processes that include some of the latest machines and deep learning methods, providing an unprecedented solution for automating this task. Nevertheless, the correlation between routing-induced parasitic structures and functional behavior of circuit switches is beyond simple, computationally intensive and layout-oriented synthetic techniques in which automatic routing techniques play a critical role.

#### **III. PROPOSED METHODOLOGY**

Circuit routing issues consider the study of routing algorithms. Architectures that learn depth like deep neural networks, deep faith networks, repeating neural networks, folding networks, and transformer use human experts. [3] [4] [5] Deep learning algorithms show prominent services in a variety of tasks, but are susceptible to the reinforcement of heirs and biases present in training data. This can manifest in distorted representations and unfair treatment of various demographics, such as: B. Based on breed, gender, language, [6] and cultural groups. Anne has a different difference from the organic brain. In particular, artificial neural networks tend to be static and symbolic, but most organisms' biological brains are dynamic (plastic) and analog. [7] [8] ANNs are generally considered as a low-quality model of brain function. Run a simulation of the game tree to find the best behaviour. In the tree, the simulation starts with the root node representing the game status by creating a subordinate node representing the new state information. As shown in Figure 3, MCT is performed as a four-stage process. In this process, the upper reliability of the upper



reliability is used as a way to select the lower node. The subknot becomes the node of the leaf in the tree. The best child will be returned.

#### **IV. SIMULATIONS AND RESULTS**

Here discussed the study of routing algorithms. Additionally, routing methods have been introduced, using AI technology. DRL can act as a manufacturer of the best choice decisions in a variety of dynamic problems. Therefore, it is used in a variety of AI-based enhanced routing technology is also presented to improve routing performance.



Figure 1:"Hybrid AI-based circuit designer" Flow chart

It can be seen that circuit routing performance differs based on performance. Use a small range to send data for bandwidth. Here, data transfer times and long delays are significantly reduced as data transmissions can occur at the switching nodes latency. The performance of the low arithmetic complexity of these algorithms is efficient.

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Fig. 3 Graph of Link utilization versus  $\lambda$ .

#### V. CONCLUSION

The results demonstrate that our strategy reduces the load distribution rather than reduce the overall burden on the network. Finally, consistent results are achieved through simulation results. This is a strategy that presents a PCB.



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Several tests have been conducted to use these MCT-based AI technologies in PCB routing algorithms. The guidelines for selective node extension of MCTs prevent us from observing enough nodes to accurately assess long-term outcomes with many combination problems. Therefore, there is a better routing path with some line routing issues than what we discussed in the MCTS process.

#### REFERENCES

[1]C.-X. Lin, C.-H. Liu, I.-C. Chen, D. Lee, and T.-Y. Ho, "An efficient bi-criteria flow channel routing algorithm for flow-based microfluidic biochips," in Design Autom. Conf., 2014, pp. 1-6.

[2] K. Hu, T. Dinh, T. Y. Ho, and K. Chakrabarty, "Control-layer routing and control-pin minimization for flow-based Microfluidic Biochips," Trans. Comput.-Aided Design of Integr. Circuits Syst., vol. PP, no. 99, 2016.

[3] Q. Wang, H. Zou, H. Yao, T.-Y. Ho, R. Wille, and Y. Cai, "Physical codesign of flow and control layers for flowbased microfluidic biochips," Trans. Comput.-Aided Design of Integr. Circuits Syst., vol. 37, no. 6, pp. 1157-1170, 2017.

[4] Y. Zhu et al., "Multi-channel and fault-tolerant control multiplexing for flow-based microfluidic biochips," in Int'l Conf. Comput.-Aided Design, 2018.

[5] X. Chen and C. L. Ren, "A microfluidic chip integrated with droplet generation, pairing, trapping, merging, mixing and releasing," RSC Adv., vol. 7, no. 27, pp. 16738-16750, 2017.

[6] X. Li, D. R. Ballerini, and W. Shen, "A perspective on paper-based microfluidics: Current status and future trends," Biomicrofluidics, vol. 6, no. 1, p. 011301, 2012.

[7] J. Guerrero, Y.-W. Chang, A. A. Fragkopoulos, and A. Fernandez-Nieves, "Capillary-based Microfluidics-Coflow, flowfocusing, electro-Coflow, drops, jets, and instabilities," Small, vol. 16, no. 9, p. 1904344, 2020.

[8] P.-H. Yuh, C.-L. Yang, and Y.-W. Chang, "BioRoute: A networkflow- based routing algorithm for the synthesis of digital microfluidic biochips," Trans. Comput.-Aided Design of Integr. Circuits Syst., vol. 27, no. 11, pp. 1928–1941, 2008.

[9] O. Keszocze, R. Wille, and R. Drechsler, "Exact routing for digital microfluidic biochips with temporary blockages," in Int'l Conf. Comput.-Aided Design, 2014, pp. 405-410.

[10] O. Keszocze, R. Wille, K. Chakrabarty, and R. Drechsler, "A general and exact routing methodology for digital Microfluidic Biochips," in Int'l Conf. Comput.-Aided Design, 2015, pp. 874-881.



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