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Transmission and Reception Strategies for a Hybrid Optical Fiber-FSO System with Advanced Data Serialization Techniques

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ABSTRACT: The exponential growth of wireless transceivers necessitates extremely fast data transmission at a high level of service, which optical fibre and Free Space Optics (FSO) can provide. As the demand for data transfer increases and new technologies become available, novel research must be conducted to combine the benefits of both technologies. Optical communication technologies serve as the backbone of wireless technology in this instance. Currently, only a few studies on various transmission reception methods for Free Space Optical (FSO) communication using Field Programmable Gate Arrays have been conducted. The primary objective of this paper is to identify research trends and emerging themes in the development of FPGA-based Optical Hybrid Fibre - FSO Communication Systems over the last decade. When used in conjunction with a variety of data transmission and reception technologies and data serialization approaches, this paper demonstrates the reliability and compatibility of FPGA-based FSOs. This FPGA-based FSO is intended for optical communication applications requiring highly secure transmission schemes, low radiation noise, a low bit error rate, and a high data transfer rate.

KEYWORDS: FPGA, FSO, OFDM, DWDM, BER, OSNR, PON

I. INTRODUCTION

Future networks are projected to provide broadband services while also enabling mobility. Thus, radio over fibre or fibre wireless integration, which combines the benefits of broadband (optical communication) and mobility (wireless communication), has been viewed as a possible alternative for future access networks. Due to the rapidly growing need for bandwidth and download speed, technologies capable of achieving multi-gigabit connection speeds have garnered considerable interest in recent years in order to improve availability, data rates, and services. Optical communication systems, such as the Free Space Optical (FSO) Communication System, combine the advantages of radio frequency (RF) and microwave wireless technologies in a single system.

The increased transmission distance expands the optical access network's coverage, which reduces the cost of optical communication systems. As demand for high-speed data services continues to grow, additional bandwidth in the access network is required. In any case, while standard wavelength division multiplexing-based Passive Optical Networks (PONs) are a possible solution, but the associated electrical and optical components may be prohibitively expensive. Recently, optical orthogonal frequency-division multiplexing (OFDM) with intensity modulation and direct detection (IM/DD) has been widely regarded as a promising candidate technology for next-generation PONs (NG-PONs) beyond time- and wavelength-division multiplexed (TWDM) NG-PONs, due to its simplicity in comparison to coherent optical OFDM (CO-OFDM) NG-PONs. Additionally, it incorporates advanced digital signal processing technologies, a high efficiency of spectrum use, good resistance to dispersion defects, and simple frequency-domain equalization.

Meanwhile, OFDM-based PON can support dynamic bandwidth allocation in both the time and frequency domains, as well as be compatible with existing PONs. To further increase transmission capacity or spectral efficiency (SE) and to reduce the bandwidth requirements of electronic components in both transmitters and receivers, one of the most cost-effective approaches is to use a high-level modulation format such as quadrature amplitude modulation (QAM) on the data-carrying subcarriers of OFDM symbols.

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Due to its increased signal integrity and fast transmission speeds, serial transmission technology is increasingly being adopted for digital data transmission. Serial interface components have a number of advantages over parallel interface components. Both of the aforementioned technologies have been thoroughly investigated in this paper.

II. TECHNOLOGY COMPARISONS

A. Transmission and Reception Methodology Comparison

Intra- and inter-data centre traffic is growing at a rapid pace, and there is a high demand for bandwidth, particularly in access and metro areas. By 2020, voice and data traffic on the Internet is expected to reach 1 Peta bit/s. These growth prospects imply that performance requirements for new optical systems will continue to rise. These requirements apply to the fibres and devices themselves, as well as the network and transceiver architectures and access protocols. As a result, the incorporation of several novel technologies into future equipment deployment is a foregone conclusion. Different transmission reception methods contribute to next-generation cost effective high-speed transceivers. This becomes interest for not only long-haul but also access networks applications due to advantages such as adaptive bandwidth usage and different modulation format capability per subcarrier.

The purpose of the paper [1] is to demonstrate the feasibility, performance, and circuit size of a fully functional 112-Gbit/s single-carrier 16QAM/16APSK transceiver based on an FPGA. Additionally, it includes the first real-time hardware implementations of two critical functions, the Rx-side phase noise and the chromatic dispersion (CD) cancellation circuits (MSPE and 1-sps CD compensation), for the purpose of improving the performance of a delay-detection-based optical multilevel transceiver. The article [2] describes how to create the front-end of a single-carrier coherent optical receiver for optical networks using an FPGA. The receiver employs a variety of spectrally efficient approaches, including polarization multiplexing and 16-QAM modulation. The FPGA implementation was validated using received traces (time series) derived from optical simulations for 112 Gb/s channel data rates. Future study will concentrate on using efficient error control coding to improve the optical receiver's BER performance. Paper [3] demonstrates a real-time FPGA implementation of a coherent optical OFDM transmitter and receiver. It is implemented utilizing two 2.5 GHz DACs and one FPGA for the transmitter, two ADCs and one FPGA for the receiver, and real-time digital signal processing based on FPGAs for coherent optical OFDM transmission. At the receiver, QPSK modulated OFDM signals are recovered effectively. The proposed OFDM system in the paper [4] features a low-cost hardware architecture that includes Quadrature Amplitude Modulation (QAM) modulation-demodulation, highly pipelined Inverse Fast Fourier Transform (IFFT)-Fast Fourier Transform (FFT) modelling, and digital conversion systems such as Direct Up-Conversion (DUC) and Direct Down-Conversion (DDC), which support real-time requirements for RF systems. The proposed OFDM systems are capable of transmitting both data and images. The suggested approach achieves the desired result by reducing the area overhead, overall power consumption, and hardware complexity of OFDM systems on FPGA chips. The article [5] presents the design and implementation of an OFDM transceiver using an FPGA. The system is designed in VHDL, produced using a high-level synthesis tool, and optimized for the Xilinx platform. This paper also discusses the resources required for the transmitter and receiver. The architecture makes use of Xilinx's IP cores for floating point multiplication, addition, subtraction, and division. The IFFT and FFT are calculated using the DIT radix-2 butterfly technique. Additionally, by increasing the number of subcarriers and implementing a highly pipelined design for IFFT and FFT, system performance in terms of processing time required in the transmitter and receiver might be increased. The article [6] demonstrates the first real-time adaptive 4-64 QAM optical coherent transmission system using an OPLL technique and an FPGA-based transmitter and receiver. Over 320 kilometers with an optical bandwidth of 6 GHz, polarization-multiplexed 5 Gsymbol/s, 4-64 QAM (20-60 Gbit/s) signals were transmitted. In future work, a simpler system will be implemented using FPGA-based polarization and clock recovery circuits, allowing us to reduce the system's tonal count. Additionally, the four FPGAs for parallel processing can be implemented on the SoC. For the first time, stage-dependent clipping of FFT DSP operation dynamic range is proposed and extensively investigated in the paper [7], based on which an improved stage-dependent minimum bit resolution map is numerically identified by taking into account FFT DSP operation dynamic range-clipping and precision. In 25km SSMF OOFDM transmission systems based on intensity modulation and direct detection, the validity and high accuracy of the selected minimum bit resolution map is experimentally validated (IMDD). The FFT architecture is capable of fully using all complex multiplication processes. This suggests that decreasing the bit resolution of the FFT DSP operation is the most effective technique for minimizing the FFT DSP logic resource utilization effectively. A real-time 10 Gbit/s-QAM (2.5 Gsymbol/s, 16 QAM) QSC (Quantum Stream Cipher) transmission over 320 kilometers was realized in [8] using an FPGA-based transmitter and receiver. After a 320km transmission, an error-free operation for a legitimate receiver (Bob) can be achieved by maintaining a detection failure probability of more than 99.93 percent for Eve. By utilizing all optical devices such as optical amplifiers at intermediate distances, transmission distance and quality can be increased further. The creation of a 10.4-Gb/s net-rate

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single-band real-time IM/DD optical OFDM receiver based on a field programmable gate array is described in the letter [9]. The performance of receiving a 10.4-Gb/s adaptively modulated 256/64/16QAM-encoded optical OFDM signal with a high SE of 4.84-bit/s/Hz that was generated off-line is investigated. In addition, the ideal threshold value for the fundamental training sequence-based symbol synchronization is investigated in the high-speed real-time receiver. A suitable method can be used to address the modest power penalty for the real-time receiver. The study [10] proposed a coherent ultra-dense wavelength division multiplexing passive optical network (UDWDMPON) architecture for symmetrical operations between the uplink and downlink. Show a field trial of coherent UDWDM-PON using real-time field programmable gate array (FPGA)-based transceivers. The optical distribution network power budget for this system is computed utilizing 40 C band downlink UDWDM channels with a 5 GHz channel spacing. After transmission via a 40-kilometer field-installed fiber connection, the experimental demonstration can achieve power budgets of 29 dB employing dual-polarization quadrature phase-shift keying formats. But it is necessary to address the issue of complexity reduction. The paper [11] developed a Twin-SSBOFDM W-band fiber-wireless transmission system using optical heterodyne creation and RF heterodyne detection. Meanwhile, based on FFT and MDIF&MAF, the paper provides a simple blind carrier recovery strategy. A 12-GSa/s two-channel AWG transmitter and a 25-GSa/s DSO receiver are used in an offline experiment to evaluate the system's performance. When conducting carrier recovery in an FPGA, using additional parallel channels can be tried. The study [12] uses a Centralized Light Source (CLS) configuration to show real-time digital service and multimedia service upstream transmission in a Digital Signal Processing (DSP)-based Orthogonal Frequency Division Multiplexing-Passive Optical Network (OFDM-PON). The Bit Error Rate (BER) is 9.5x 10^{-11} after transmission over 25 km of Standard Single Mode Fibre (SSMF) with -16.5 dBm optical power at receiver. The use of a Field Programmable Gate Array (FPGA) to implement digital domain up-conversion and down-conversion reduces the expense of in-phase and quadrature (IQ) radio frequency mixers used at the transmitter and receiver. Using this technology, the transmission distance can be increased to more than 100 kilometers. The article [13] discusses a novel Field Programmable Gate Array (FPGA) technique for gaining an advantage in the implementation of OFDM systems. Current and future communication schemes frequently employ OFDM systems to achieve high baud rates, low inter carrier interference (IC), and low inter symbol interference (ISI). This article describes the design, validation, and implementation of an OFDM modulator for IEEE-802.16e using an FPGA and a high-level design tool like VHDL. Numerous novel techniques have been developed over the years to address the design challenges associated with OFDM-based FPGAs. The article [14] discusses the design and implementation of an OFDM-based WLAN receiver on an FPGA. The circuit is customized to comply with IEEE 802.11a/g standards. Frame detection, time and frequency synchronization, demodulation, equalization, and phase tracking are all included in the system. The algorithms that will be used to accomplish each task are chosen based on their performance, hardware cost, and latency. Additionally, each algorithm is subjected to a fixed-point analysis. Numerous algorithms in addition to CORDIC have been developed over the years used to carry out the functions specified in this work. The article [15] reviews the progress made in ultra-dense wavelength division multiplexing passive optical networks (UDWDM-PONs) by examining the technology's key characteristics in the context of optical access and metro networks. Apart from the inherent properties of coherent technology, this chapter discusses various modulation formats and pulse shaping. Experiments with a 12 x 10 Gb/s bidirectional UDWDM-PON over a hybrid 80 km standard single mode fiber (SSMF) and optical wireless link demonstrate the performance. The tests make use of a high-density, 6.25 GHz grid, Nyquist-shaped 16-ary quadrature amplitude modulation (16QAM), and digital frequency shifting. Future work will focus on demonstrating real-time operation of the transmitter and receiver for higher order modulation formats and flexi-grid multi-channel systems. To achieve high reliability receiving performances, an adaptive terminal dispersion compensation and demodulation scheme based on a dual-feedback strategy is proposed in [16] for 40 Gbps return-to-zero differential quaternary phase shift keying (RZ-DQPSK) fiber communication receivers. The balanced receiver feedback and frame error rate are both used in this paper's receiving system to achieve accurate RZ-DQPSK optical signal demodulation and adaptive dispersion compensation. The paper [17] describes the first on-line 256QAM digital coherent optical transmission system using an ECLD light source and DFB LD-based injection-locking, as well as an FPGA-based transceiver. Precision optical phase control was achieved in this system using an optical injection-locking circuit and a phase-locked loop circuit at the receiver, which helped to reduce the complexity of the FPGA-based receiver's digital signal processing. In the future, mobile front haul (MFH) operations will incorporate wireless communication, allowing for the use of a novel optical-wireless linked modulation and coding scheme to reduce the FEC processing time during MFH transmission. The current system is expected to be used for high-capacity MFH in the future. The paper [18] presents a demonstration of a power-efficient coherent interleaved frequency domain multiple access passive optical network (IFDMA-PON) uplink system. The coherent IFDMA-based quadrature phase-shift keying (PSK) digital signal processing circuits are implemented on 40-nm field programmable gate arrays. The optical network unit's power consumption is reduced to one-tenth that of conventional orthogonal frequency-division multiple access-PON systems by utilising polar-coordinate transformed mapping of the PSK signal. This can be combined with the advantages of OFDM in future systems. The paper [19] describes in detail the recent

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demonstration of a secure physical layer transmission rate of 10 Tbit/s using a digital coherent QAM quantum noise stream cypher (QNSC) and injection-locked WDM techniques. A FPGA-based transmitter and receiver are used to demonstrate a 165-channel polarization-multiplexed WDM 5 Gbaud 128 QAM/QNSC (70Gbit/s) on-line transmission over a distance of 160 km with a spectral efficiency of 6 bit/s/Hz. The original 128QAM data was encrypted in this system using basis information in a 1024x1024 QAM format. By increasing the FEC strength, the masking noise level at the transmitter and the density of the WDM signal can be increased, resulting in an increase in both the number of masked signals and spectral efficiency. It is demonstrated that the generation and reuse of a self-pulsated optical RZ carrier enables bi-directional OC-768 transmission at 40 Gbit/s using downstream return-to-zero binary phase-shift keying (RZ-BPSK) and reused upstream return-to-zero ON–OFF keying (RZ-OOK) in [20]. The self-started optical RZ carrier is generated by coupling a single-mode laser to a self-feedback loop based on a nonlinearly biased Mach–Zehnder modulator that is externally modulated to transmit the downstream RZ-BPSK and reused to transmit the upstream RZ-OOK. In the future, self-consistent very high-speed TDM communication links operating at even higher frequencies can be implemented at a very low architectural cost. This is also extendable to FDM and CDM technologies. The letter [21] describes a 65-nm Si-CMOS-based on-off keying (OOK) receiver with high speed and low power consumption. Because of the wide-bandwidth circuitry, the receiver uses OOK modulation for low power consumption and runs at a high data rate. A wideband low-noise amplifier (LNA), a gain-boosting detector, and a third-order active feedback amplifier make up the receiver. For a 2^7-1 pseudorandom binary sequence (PRBS), the receiver reaches 20 Gb/s with a bit-error rate (BER) of less than 10^{-11}. This receiver is suitable for the next generation of wireless interconnect. Bi-directional down-stream RZ-BPSK and up-stream reusable RZ-OOK transmissions at 10-Gbit/s is described in [22] using a self-started DFBLD-EAM pulsed carrier at 10 GHz. The self-pulsating DFBLD-EAM is driven by a fiber true-time-delay integrated self-feedback optoelectronic oscillator (OEO) in the central office to deliver a pulsed RZ carrier source. The pulse width and jitter of the self-started RZ-BPSK carrier are theoretically and empirically adjusted with the true-time-delay included OEO feedback loop with the lowest SSB phase noise. In the hybrid BPSK-OOK transmission network, this self-pulsating EAM RZ carrier and its reuse capability can be utilized in future systems. The study [23] presents an 11.3 Gbps CMOS SONET compatible transceiver that supports both RZ and NRZ data formats. The transmitter may alter output format between RZ and NRZ using a programmable high-speed transmit channel with an AND gate and a duty cycle adjustment circuit. Multi rate and multiformat operation modes will give next-generation mainstream optical transceivers more versatility. The first demonstration of 640-Gb/s return-to-zero ON–OFF keying channel transmission using midspan phase conjugation over a 100-km standard single-mode fibre link is presented in this paper [24]. For the first time, a frequency-degenerate conjugate field spanning more than 20 nm is generated in a low-birefringence parametric mixer. The use of a high-quality 640-Gb/s transmitter and a high-sensitivity receiver demonstrated error-free (bit error ratio 10^{-9}) performance, eliminating the requirement for prohibitive fiber length control or electronic signal processing. This technique has the potential to be scaled up to a fiber transmission distance of 1000 kilometers. A single-carrier 800-Gb/s coherent transmission of polarization-multiplexed 32 return-to-zero (RZ)/ quadrature amplitude modulation signals at 10 Gsymbol/s 8 optical time-division multiplexing signals at 10 Gsymbol/s (OTDM) is presented in the paper [25]. The RZ-continuous-wave conversion system was used in a coherent receiver to demodulate and demultiplex ultra-high-speed multilevel OTDM signals with a high signal-to-noise ratio, allowing transmission across 225 km. This technology is likely to be especially useful in the Tbit/s region for greater multiplicity coherent OTDM transmission.

Diverse transmission reception techniques contribute to the development of next-generation low-cost high-speed transceivers. Future research will concentrate on the incorporation of effective error control coding in order to improve the BER performance of optical receivers. It is possible to implement adaptive bandwidth consumption and multiplexing methods such as DWDM. The benefits of OFDM can be combined with the suggested modulation techniques to improve data transmission speed and bandwidth efficiency, but the hardware requirements for OOK modulation are lower and implementation is simpler. OSNR, Q factor, Data rates and Link distances can also be analysed from this study.

Table 1 Comparison of data transmission rate and transmission distance results of various Transmission-Reception methods

REFERENCE NO:	YEAR	DATA TRANSMISSION RATES (Gbps)	DISTANCE (km)
23	2011	11.3	25

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24	2011	640	100
22	2012	10	25
25	2012	800	225
16	2013	40	63
18	2014	6	20
12	2014	1	25
9	2014	10.4	20
6	2014	60	320
15	2015	10	80
1	2015	448	18.2
8	2015	10	320
11	2018	40.7	22
10	2019	10	40
17	2020	80	10

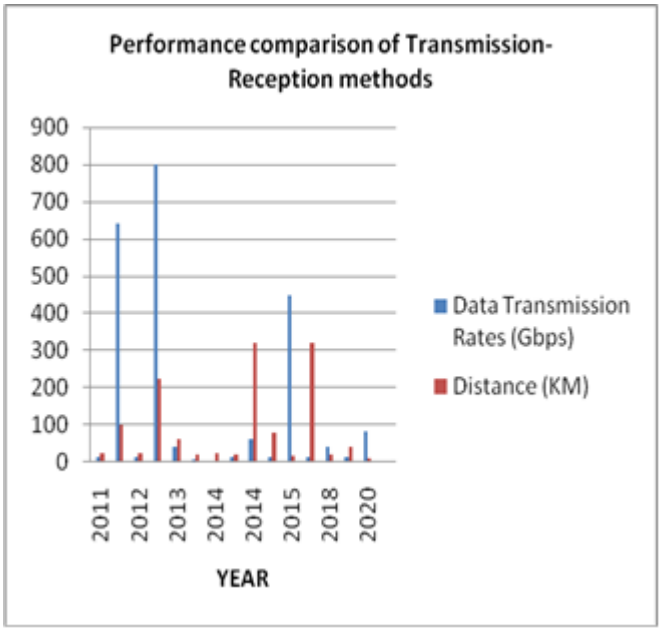

Fig. 1 The progress of data transmission rate and transmission distance with multiple Transmission reception formats

B. Comparison of data Serialization techniques

Serial Peripheral Interface (SPI) is a widely used communication protocol that enables serial data transfer over a short distance between a master and a slave device. The mission management computer, which is the central processing unit of the comprehensive task processing system, is in charge of the system's operation, including data processing, information processing, and data decoding. It communicates with other equipments via a variety of different communication protocols. While the majority of interface options adhere to industry-standard protocols such as RS232, RS422, RS485, ARINC429, and simulation, some devices have unique requirements. To ensure that regular communication functions, it is necessary to design a private communication interface. The standard module is critical because it ensures the system's stability and reliability. Additionally, it reduces design staff effort and significantly increases efficiency.

The article [26] discusses the FPGA-based private communication interface and how it can be used to extend the functionality of an existing module without requiring additional hardware. This article describes the effective design of

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a low-cost SerDes link for sending/receiving SPI and GPIO data using a low-cost CLPD/FPGA, utilizing the chip's resources efficiently and minimizing any difficulties with latency. A Serializer/Deserializer (SerDes) pair is a pair of functional blocks that are frequently employed in high-speed communications to compensate for restricted input(s)/output(s). Additionally, it is demonstrated that when latency is a concern over a long distance, this technique successfully resynchronizes the MISO line, which is not achievable with any hardware solution. The paper [27] describes the design of a serial communication interface based on an FPGA (Field Programmable Gate Array) for data connection with other devices. It ensures that the serial communication function is implemented without requiring an increase in hardware resources. It adheres to the notion of standardization of hardware equipment. The design method for the private serial interface based on FPGA is demonstrated in this article; it has enabled the realization of new functions, shortened the development cycle, reduced manpower investment, and adhered to the module standardization principle in the case of without increasing the original module kind. This design technique is one that should be promoted in future design. The article [28] discusses the construction of a fiber channel-based communication protocol on an FPGA for use in avionics. Fiber channel technology is extremely efficient in avionics applications. This study proposes a framework for fiber channel-based communication protocol receiver implementation on FPGA based on the Fiber Channel – Avionics Environment (FC-AE) protocol. The receiver is integrated into the project's work. The findings illustrate the receiving of a data frame on the FPGA and its transmission to the host. The communication system has a maximum speed of 2.5Gbps. This article [29] investigated the usage of the mother LDPC code in conjunction with SD decoding in order to further improve the performance of forward error correction (FEC). It is discovered that this technique provides 1.3 dB more gross coding gain than that specified in the IEEE 802.3ca 25G-EPON standards, based on experimental measurements using a real-time FPGA platform. With this enhanced SD-LDPC performance, it is able to sustain a link budget of PR30 (29dB) for 50GPON.This article [30] proposes a design and implementation of a high-speed serial data transmission system capable of transmitting 128-bit data at a rate of 3.125Gbps, utilizing the architectural features of the virtex-5 FPGA. The Aurora protocol is used for data transmission and reception on Multi-Gigabit Transceivers (MGT's). The 128-bit parallel data generated by a counter is transmitted to the aurora module via asynchronous first-in-first-out (AFIFO). The FPGA's multi-gigabit transceivers are configured using the Aurora protocol and operate at a 156.25 MHz clock rate (MGT clock). The Aurora protocol converts serial to parallel data and vice versa. Serial Rapid IO (SRIO) is the next level protocol, which operates on the principle of data packet switching. It is more efficient for error-free transmission and allows for increased speed.

The solutions should ensure that the serial communication function is realized without requiring additional hardware resources or module function expansion, while also shortening the development cycle, reducing manpower expenditure, and meeting module standards requirements. This is appropriate for situations requiring high-speed continuous conversion. The conversion rate of the module should be quite low, and the amount of data should be quite minimal. This method is straightforward and ideal for low-speed and low-data situations, and it can be used to provide serial interface AD/DA control. One of the disadvantages is the limited data transfer speed. The primary benefit of integrating SPI and SerDes is the ability to transmit and receive SPI signals over long distances. It is capable of implementing a low-cost SerDes link for sending/receiving SPI and GPIO data using a low-cost CLPD/FPGA, utilizing the chip's resources efficiently and minimizing any concerns with latency.

III. PROPOSED SYSTEM

The proposed system implementation block diagram is depicted in Figure 2. The block diagram provides a more comprehensive and clear representation of the hybrid transceiver's functionality incorporating data serialization.

- Data Source: Generates the data to be transmitted.
- Data Serialization & Framing Unit: Converts the data into a suitable format for transmission. This includes packetization or framing, adding headers, and sequence numbers.
- Switching Control Unit: Decides whether to use the FSO or Fiber path based on channel conditions or other criteria. This unit monitors the quality of the FSO link (e.g., received signal strength, BER) and makes the switching decision. It also controls the switches that direct the data to the appropriate path.
- FSO TX Path:
    - FSO Modulation: Modulates the data onto the optical carrier using a suitable modulation scheme (e.g., OOK, PPM, QAM).
    - FSO Laser Driver: Drives the FSO laser (e.g., VCSEL) to generate the optical signal.
    - FSO Optics: Includes lenses and mirrors to focus and direct the FSO beam.
    - FSO Channel: The atmospheric path through which the FSO signal propagates.

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- Fiber TX Path:
  - Fiber Modulation: Modulates the data for fiber transmission (e.g., NRZ).
  - Fiber TX Optics: Includes the laser or LED source and associated optics for launching the signal into the fiber.
  - Fiber Optic Connector: Connects the transceiver to the fiber optic cable.
  - Fiber Optic Cable: The physical medium for fiber optic transmission.
- FSO/Fiber Receiver:
  - FSO/Fiber Receiver (Photodiode): Detects the optical signal.
  - FSO/Fiber Demodulation: Demodulates the received optical signal to recover the data.
  - Error Correction & Detection: Performs error correction (FEC) and error detection (CRC) to improve data reliability.
- Data Deserialization & Defaming: Reverses the serialization and framing process to recover the original data.
- Data Sink: The destination of the received data.

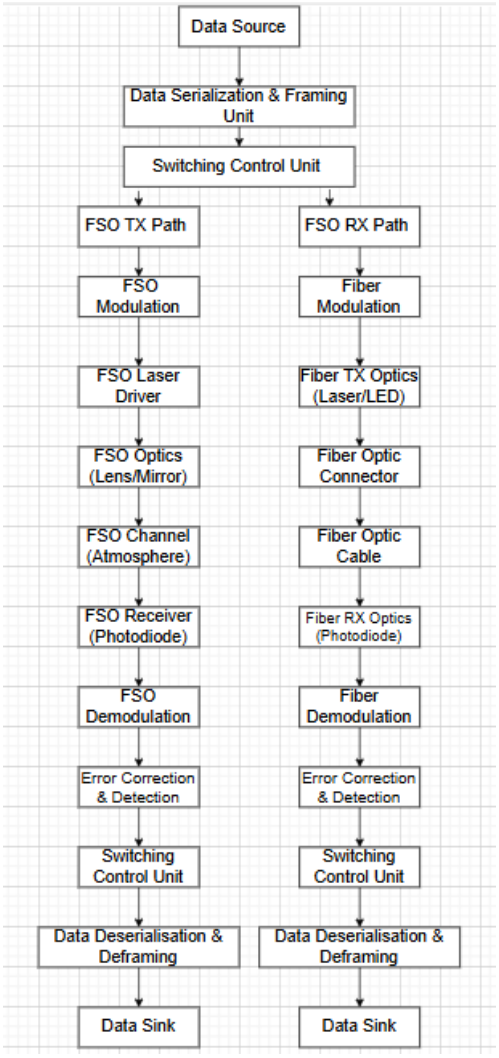

Fig. 2 The proposed block diagram for a Hybrid FSO – FIBER Transceiver with data serialization

IV.CONCLUSION

Currently, only a few studies on FSO communication transceivers using FPGAs and data serialization have been conducted. These published studies are exceedingly convoluted and fragmentary. Currently, the FPGA is used as a modem for optical communication systems, digital signal processing systems, and computer data transmission. FSOs

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based on FPGA chips can also reduce power consumption while keeping a low-cost structure. Because of its reliability, several researchers want to develop FPGA-based FSO systems. However, a modest study is being conducted to compare the advantages of FPGA and FSO. This work compares several transmission and reception methods, as well as data serialization strategies. The use of hybrid links, appropriate transmission- reception and data serialization techniques can be suggested to further push the boundaries of FSO systems. These are driven by exciting developments in FSO based on FPGA. This SLR summarizes the field's research efforts.

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