



Current Differencing Transconductance Amplifier with Improved Performance

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ABSTRACT: This paper presents, The Z copy current differencing transconductance amplifier (ZC-CDTA) is a new current-mode active element that was introduced recently. ZC-CDTA is improved from the current differencing transconductance amplifier (CDTA) and has increased its universality. In the current study, a CMOS implementation of ZC-CDTA is proposed. Which has two stages of ZC-CDTA consists of a CDU (current differencing unit) and floating current source. Demands for low voltage low power integrated circuit design are growing with technology advancement. The supply voltages are $\pm 0.9V$. This ZC-CDTA provides 540.335MHz, 692.879MHz bandwidth for respective inputs and power dissipation of 0.518mW. ASM 0.18 μm CMOS parameters are used for the simulations.

KEYWORDS: ZC-CDTA, CDTA, CCIII, current mode analog circuits.

I. INTRODUCTION

The Z copy current differencing transconductance amplifier (ZC-CDTA) is the modified version of the CDTA. ZC-CDTA has 2 low-impedance input terminals and 4 high-impedance output terminals. The inner structure of the ZC-CDTA is suitable to apply current-mode input signal and to obtain current-mode output signal. The possibility of low input impedance and high-output impedance provides an easy synthesis of current-mode active filters.

In the current study, a new CMOS ZC-CDTA structure is introduced. The topology proposed is composed of a current differencing unit, a dual output OTA, and a CCIII. The CCIII is used to copy the Z terminal current, where it acts as a floating current sensing active element.

There are number of advantages of current mode approach. This approach provides higher frequency range of operation, better accuracy rates, improved linearity and better accuracy.

The paper covers the implementation of design of positive feedback driven current-mode amplifiers z-copy CDTA and CDTA, and filter applications. The designed CDTA consumes extra low power and supply voltages in contrast to gate driven structures.

II. Z COPY CURRENT DIFFERENCING TRANSCONDUCTANCE AMPLIFIER (Z-CDTA)

ZC-CDTA (Z Copy Current Differencing Amplifier) is a new current mode active element, introduced recently as an advanced type of the Current Differencing Transconductance Amplifier. ZC-CDTA has six-ended current-mode active element. ZC-CDTA consists of two input terminal, one intermediate terminal and two output terminal. Inputs are differential and they take the difference between the currents applied to the input. This current difference is transferred to the intermediate terminal and converted to a voltage depending on external impedance. This voltage is multiplied with transconductance parameter of the operational transconductance amplifier and converted to the balance current sat output of the Z Copied Current Differencing Transconductance Amplifier. The schematic view of the ZC-CDTA is given in the Fig. 1. Furthermore, the Z Copy Current Differencing Transconductance Amplifier has additional Z terminal output, called Z copy output. The ZC-CDTA increases the universality of CDTA. The current sensing is perfectly done by the aid of third generation current conveyor. This copy of the Z terminal current provides flexibility to the circuit designer because it reflects the circuit functions at the Z output to an additional output for a further use. Such an additional terminal is especially important if the Z terminal is connected to other parts of the circuit or to passive elements which makes the current sensing difficult, since additional active elements are necessary for this

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purpose. The proposed circuit structure for the ZC-CDTA is given in Fig. 2. ZC-CDTA defining equation matrix and its basic operations formulas are given in Equation 1, 2, 3, 4, 5.

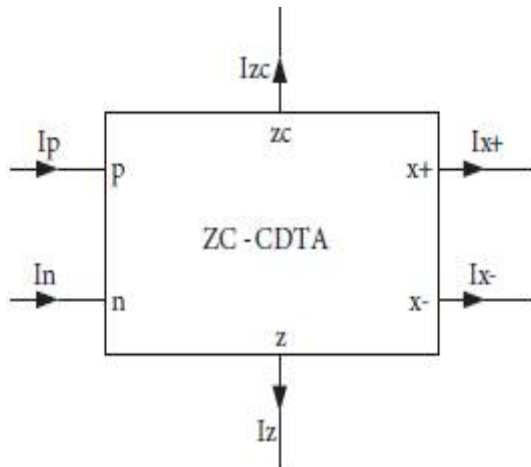


Fig. 1: Schematic view of the ZC-CDTA.

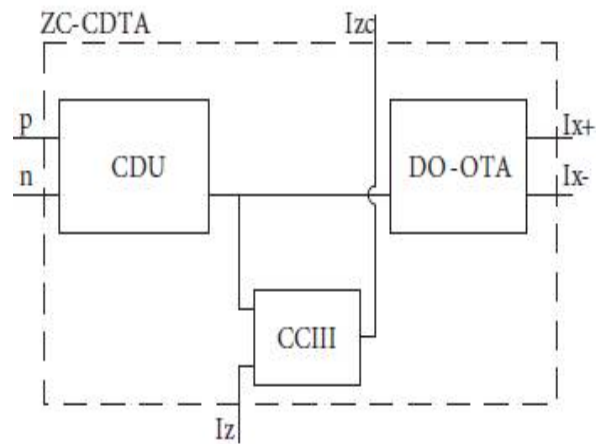


Fig. 2: Proposed circuit structure of the ZC-CDTA.

Port relation of Z-CDTA is described by following matrix.

$$\begin{pmatrix} V_p \\ V_n \\ i_z \\ i_x \\ i_{zc} \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 & 0 \\ 0 & 0 & 0 & \pm g_m & 0 \\ 0 & 0 & 0 & 0 & 0 \end{pmatrix} \begin{pmatrix} i_p \\ i_n \\ V_x \\ V_z \\ i_z \end{pmatrix} \quad (1)$$

$$V_p = V_n = 0 \quad (2)$$

$$I_z = I_{zc} = I_p - I_n \quad (3)$$

$$I_{x+} = g_m V_z \quad (4)$$

$$I_{x-} = -g_m V_z \quad (5)$$

The defining equation of the ZC-CDTA in Figure 2 becomes Eq. (6) by considering the deviation of the voltage and the current gains from their ideal values.

$$\begin{pmatrix} V_p \\ V_n \\ i_z \\ i_x \\ i_{zc} \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ \alpha_p & -\alpha_n & 0 & 0 & 0 \\ 0 & 0 & 0 & \pm g_m & 0 \\ 0 & 0 & 0 & 0 & 0 \end{pmatrix} \begin{pmatrix} i_p \\ i_n \\ V_x \\ V_z \\ i_z \end{pmatrix} \quad (6)$$

α_p And α_n are the current gains defined by $\alpha_p = 1 - \epsilon_p$ and $\alpha_n = 1 - \epsilon_n$. Here, ϵ_p and ϵ_n are current tracking errors, their absolute value is very close to zero.

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III. CMOS IMPLEMENTATION OF ZC-CDTA

The input stage of the ZC-CDTA consists of a current differencing unit. The current differencing unit CMOS structure is given in Fig. 3.

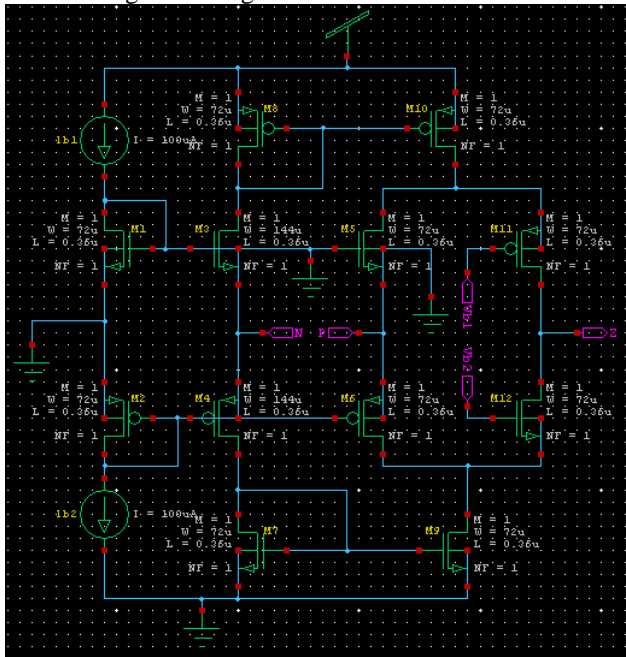


Fig. 3: The first current differencing unit CMOS structure.

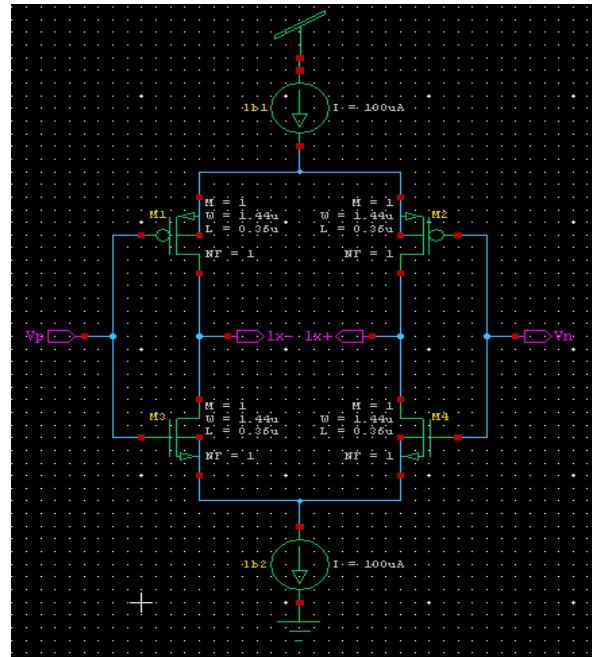


Fig. 4: The floating current source CMOS structure.

The ratios of the M3 and M4 transistors must be selected double of the M1, M2, M5 and M6 transistor ratios. Signal current is applied to the input n terminal of ZC-CDTA flows through M8 by adding M4 operating current and transferred to the M9 by current mirror. The current flowing through M3 is mirrored to M10 by the aid of M8. Signal current applied to the input p terminal of ZC-CDTA flows through M9 by adding the half of the bias current flows through M5. The half of the M4 operating current flows through M12 with the difference of p and n terminal input currents owing to M4 operating current and the n terminal current over the M9 transistor. Because of the half of M4 current over M11, the output current is the difference of the n and p terminal currents. The transistor ratios are given in Table 1.

Table 1: Transistor ratios of current differencing unit structure

Transistor	W(μm)	L(μm)
M1, M2	72	0.36
M3, M4	144	0.36
M5 - M12	72	0.36

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The bias currents of current differencing unit are selected 100 μA . The output stage of the ZC-CDTA consists of a dual output operational transconductance amplifier. The floating current source given in Fig. 4 is used for the output stage. The structure of the floating current source consists of two inverters.

The transistors ratio of the floating current source is given in Table 2. The bias currents of the floating current source are selected 100 μA .

Table 2: Transistors ratio of the floating current source

Transistor	W(μm)	L(μm)
M1 - M4	1.44	0.36

IV. SIMULATION RESULTS

The simulation results for ZC-CDTA according to fig. 3 are given in figs. 5 and 6, and the parameters of the designed Z-copy CDTA are tabulated in table 3. Fig. 5 shows the I_z/I_p curve of CDU (Current Differencing Unit) and I_z/I_n curve of CDU (Current Differencing Unit). Fig. 6 shows the Z terminal current with respect to P and N terminal. The frequency responses of I_z/I_p and I_z/I_n are 692.879 MHz and 540.335 MHz respectively.

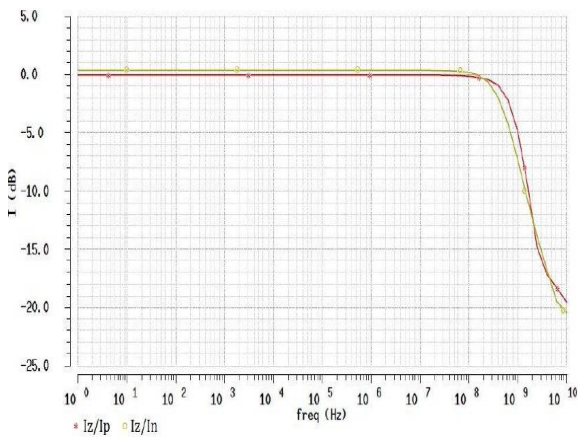


Fig. 5: Frequency responses of I_z/I_p and I_z/I_n .

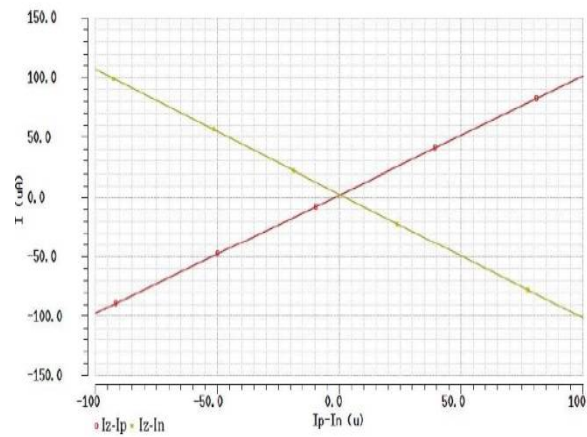


Fig. 6: Z terminal current with respect to P and N terminal.

Table 3: Simulation results of the ZC-CDTA

Supply voltage	0.9 V
Z terminal current dynamic range	$-100 \mu\text{A} \leq I_z \leq 100 \mu\text{A}$
I_z / I_n (-3dB) bandwidth	540.335 MHz
I_z / I_p (-3dB) bandwidth	692.879 MHz



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V. CONCLUSION

A new circuit configuration for realizing a ZC-CDTA in CMOS technology has been described. The main advantage of the designed ZC-CDTA is that it works on extra low supply voltage and power consumption. The 3dB bandwidth of IZ/IP and IZ/IN are 692.879 MHz and 540.335 MHz respectively. The proposed ZC-CDTA can be useful in application where extra low supply voltage is required. This circuit of ZC-CDTA plays important role in the low power filter design also. The performance of the proposed circuit is verified by cadence simulations using 0.18 μ m technology.

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BIOGRAPHY



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