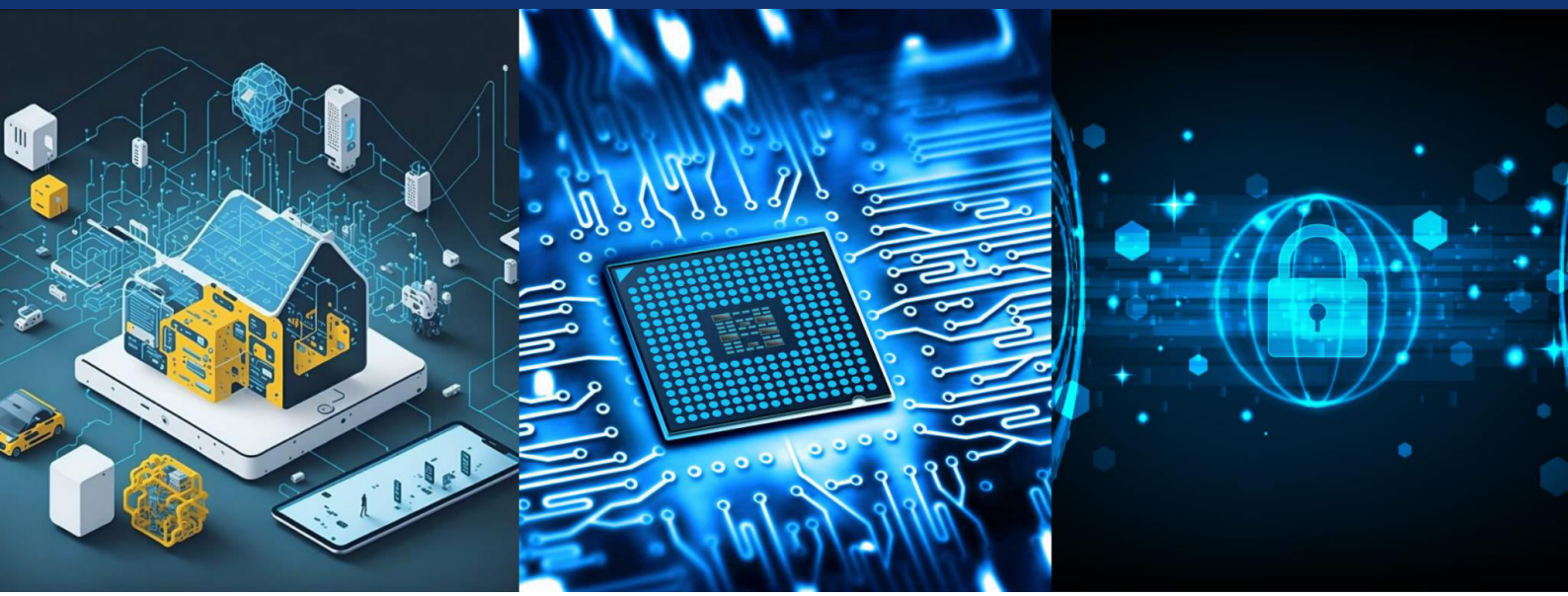
IJIRCCE

ISSN(O): 2320-9801

ISSN(P): 2320-9798



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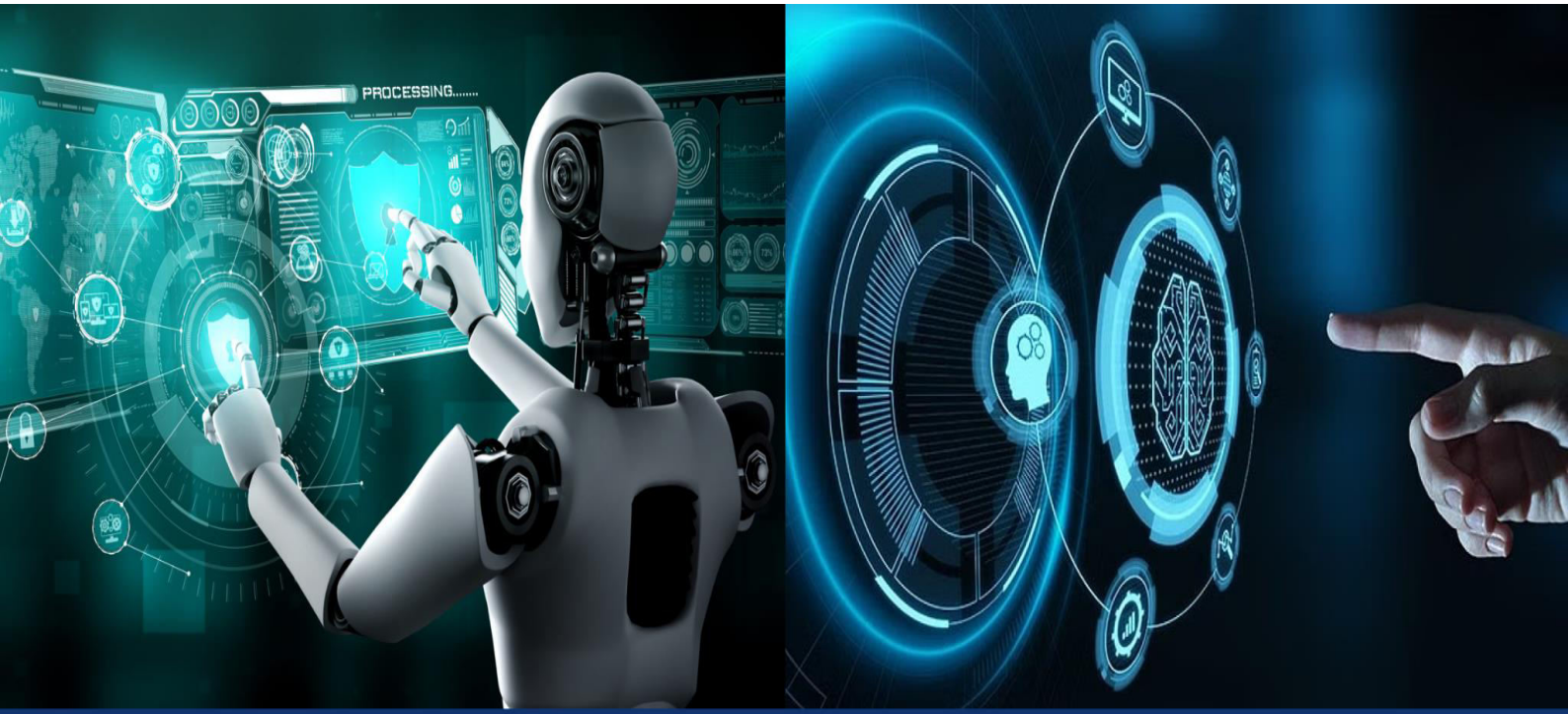

Impact Factor: 8.771

Volume 13, Issue 4, April 2025

© 2025 IJIRCCE | Volume 13, Issue 4, April 2025| DOI: 10.15680/IJIRCCE.2025.1304181

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International Journal of Innovative Research in Computer and Communication Engineering (IJIRCCE)

(A Monthly, Peer Reviewed, Refereed, Scholarly Indexed, Open Access Journal)

Performance Evaluation of 6T,7T,8T & 9T SRAM Cell Topologies at 22nm Technology Node

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ABSTRACT: SRAM (Static Random Access Memory) has become a major key component in many VLSI Chips, due to its high storage density and quick access time, it has become a popular data storage device. SRAM has played a significant role in the global VLSI sector. Due to the significant increase of low power and low voltage memory systems in recent times, SRAM has been prioritised in the research sector. This is owing to the increased demand for high-end devices, IC memory cards, and other communication devices, as well as the advancement of portable battery-operated devices. The power and area of a low power 6T,7T,8T&9T cell design are assessed in this research. This work describes the design and implementation of a 6T,7T,8T&9T SRAM cell in standard CMOS process technology at 22nm node. In the Tanner EDA Software, this simulation was run. An improvement has been obtained both in terms of Power, Area and Delay.

KEYWORDS: SRAM, Low Power Design, 22nm Technology, Tanner EDA, Power and Area Optimization

I. INTRODUCTION

The continuous scaling of CMOS technology, as predicted by Moore's Law, has driven significant advancements in Very Large Scale Integration (VLSI) design. As feature sizes shrink to the 22nm node and beyond, new challenges such as increased leakage currents, reduced device reliability, and process variations have become critical, especially in memory circuits like Static Random Access Memory (SRAM).SRAM is widely used in modern processors and System-on-Chip (SoC) architectures due to its high speed and low power consumption. However, conventional 6T SRAM cells suffer from reduced read stability, limited write margins, and higher susceptibility to noise at lower supply voltages and advanced nodes. These limitations hinder their performance in ultra-low power and high-speed applications.Advanced SRAM topologies such as 7T, 8T, and 9T have been proposed to address these issues. These designs improve robustness by modifying transistor arrangements and separating read and write paths, enhancing stability under aggressive scaling conditions. Despite occupying larger areas, these cells offer improved performance in terms of read stability, noise margins, and overall reliability. This project aims to simulate and analyze 6T, 7T, 8T, and 9T SRAM cell topologies at the 22nm technology node using Tanner EDA tools. Key performance parameters such as read and write delay, static noise margin (SNM), power consumption, and cell area will be evaluated. The comparative study provides insights into the suitability of each topology for low-power, high-performance VLSI applications, particularly in embedded systems and SoCs..

II. PROPOSED SYSTEM

The This work focuses on the design and performance analysis of 6T, 7T, 8T, and 9T SRAM cells using 22nm CMOS technology. Each topology offers different trade-offs in terms of stability, power, and performance.

6T SRAM Cell:

The 6T cell consists of two cross-coupled inverters and two access transistors. During read and write operations, the word line enables the pass transistors, allowing data transfer through the bit lines. However, simultaneous switching can cause short-circuit currents, leading to static power loss and reduced stability.

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www.ijircce.com | e-ISSN: 2320-9801, p-ISSN: 2320-9798| Impact Factor: 8.771| ESTD Year: 2013|

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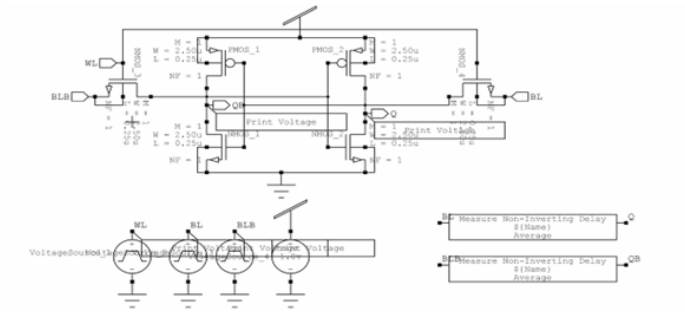

Fig.1: Schematic Diagram of 6T SRAM Cell

7T SRAM Cell:

An additional NMOS transistor is added to control feedback between the inverters, reducing power loss and improving read stability. During writing, feedback is cut off to ease data insertion, and during reading, the feedback path is reconnected for stable operation.

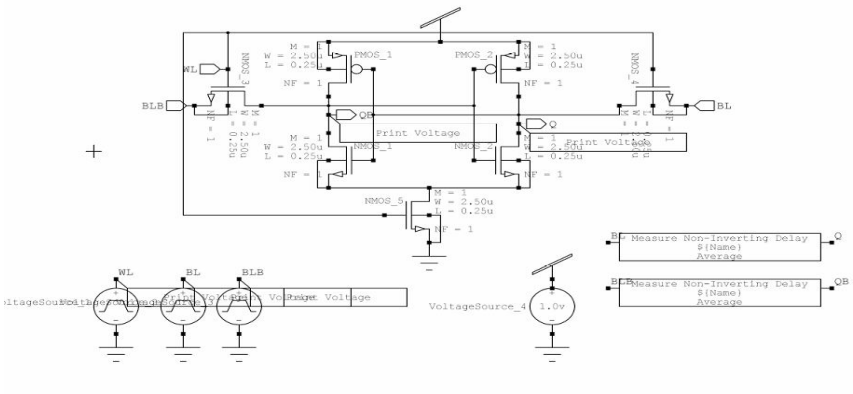

Fig.2: Schematic Diagram 7T SRAM Cell

8T SRAM Cell:

The 8T cell isolates the read and write operations by introducing separate access paths. This enhances read stability and prevents disturbance during reads. It uses precharged read bit lines and read word lines to sense data without altering storage nodes.

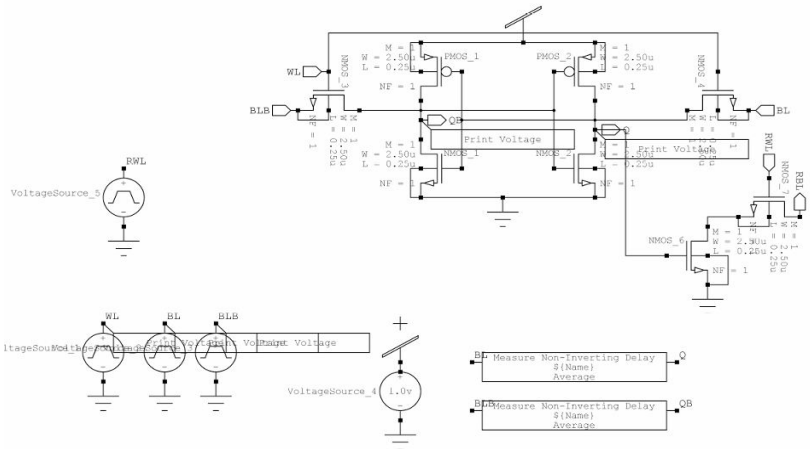

Fig.3: Schematic Diagram 8T SRAM Cell

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9T SRAM Cell:

The 9T architecture enhances data stability by decoupling read and write paths even further. It uses differential sensing and separate word lines (RWL and WWL), which significantly improves noise margins and read reliability, especially under low-voltage and variation-prone conditions. The read operation is performed through a dedicated read path that minimizes the disturbance to internal storage nodes, ensuring better robustness against bit flipping and improved sensing accuracy. Additionally, by isolating the write path, the cell becomes more tolerant to process variations and aging effects.

These designs are simulated and compared in terms of key performance metrics such as read/write delay, static noise margin (SNM), power consumption, and cell area using Tanner EDA tools. The comparative analysis under various voltage levels and process corners aims to determine the most suitable SRAM topology for modern low-power, high-performance applications.

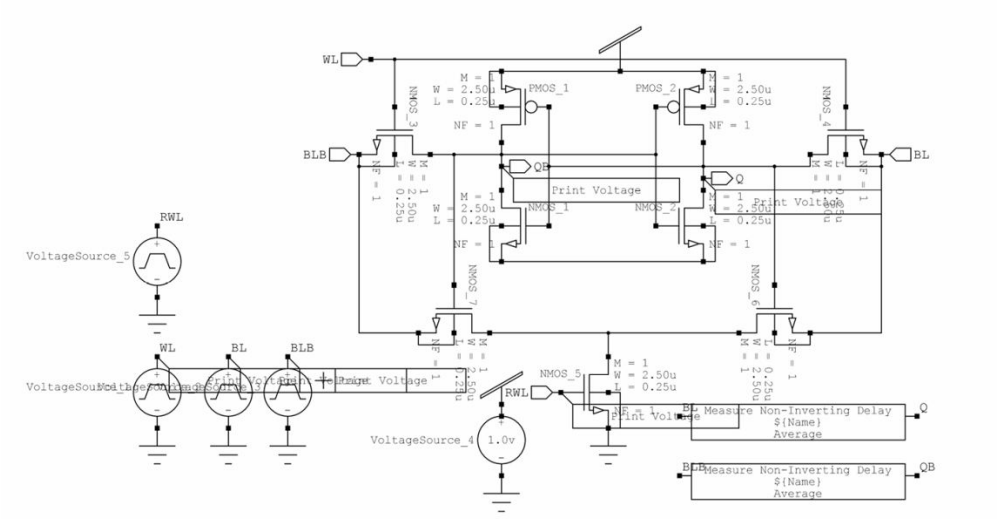

Fig.4: Schematic Diagram of 9T SRAM Cell

III. EXPERIMENTAL RESULTS

6T SRAM Cell Results:

Fig.5: Power Consumption results of 6T SRAM Cell

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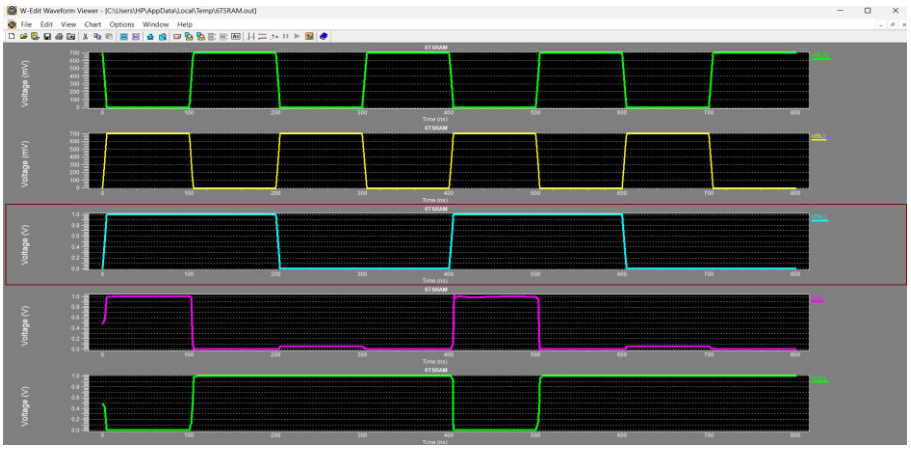
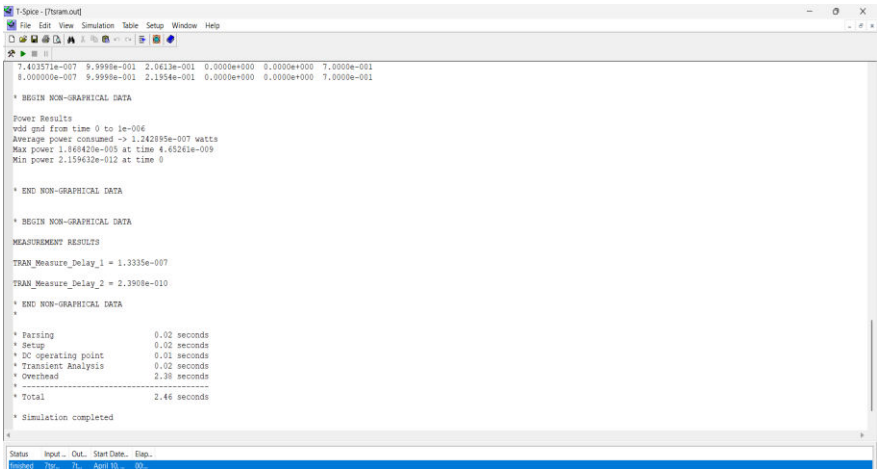


Fig.6: Simulation results of 6T SRAM Cell

7T SRAM Cell Results



```
 7.403571e-007  9.9998e-001  2.0613e-001  0.0000e+000  0.0000e+000  7.0000e-001
 8.000000e-007  9.9998e-001  2.1954e-001  0.0000e+000  0.0000e+000  7.0000e-001

* BEGIN NON-GRAPHICAL DATA

Power Results
vdd gnd from time 0 to 1e-006
Average power consumed -> 1.242895e-007 watts
Max power 1.869420e-005 at time 4.65261e-009
Min power 2.159632e-012 at time 0

* END NON-GRAPHICAL DATA

* BEGIN NON-GRAPHICAL DATA

MEASUREMENT RESULTS

TRAN_Measure_Delay_1 = 1.3335e-007

TRAN_Measure_Delay_2 = 2.3908e-010

* END NON-GRAPHICAL DATA
*
* Parsing                    0.02 seconds
* Setup                      0.02 seconds
* DC operating point         0.01 seconds
* Transient Analysis         0.02 seconds
* Overhead                   2.38 seconds
* ------------------------------------------
* Total                      2.46 seconds

* Simulation completed
```

Fig.7: Power Consumption results of 6T SRAM Cell

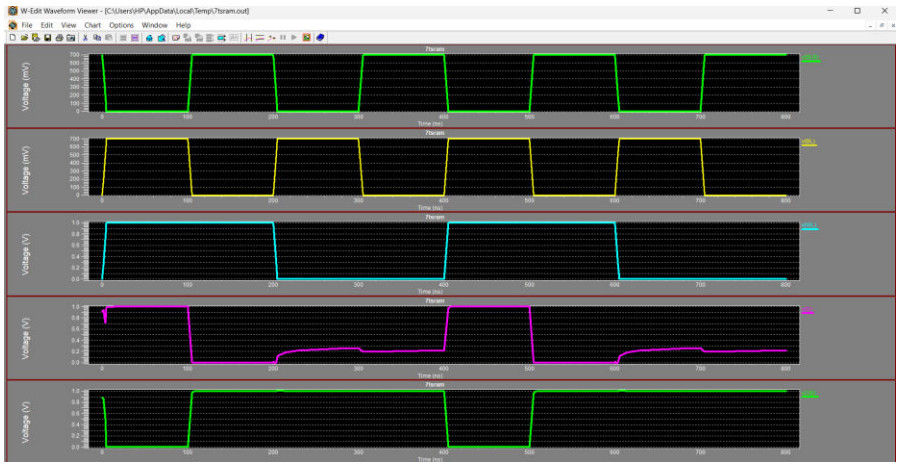


Fig.8: Simulation Results of a 7T SRAM Cell

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8T SRAM Cell Results

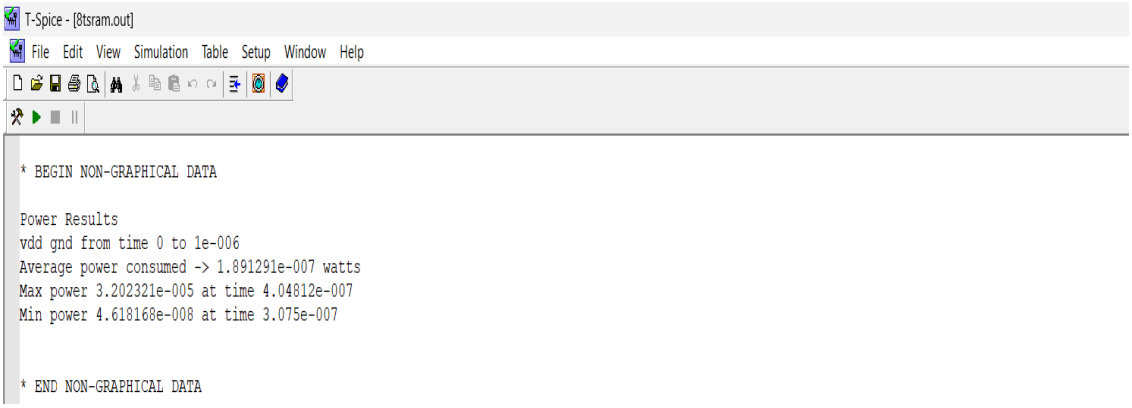

Fig.9: Power Consumption Results of a 8T SRAM Cell

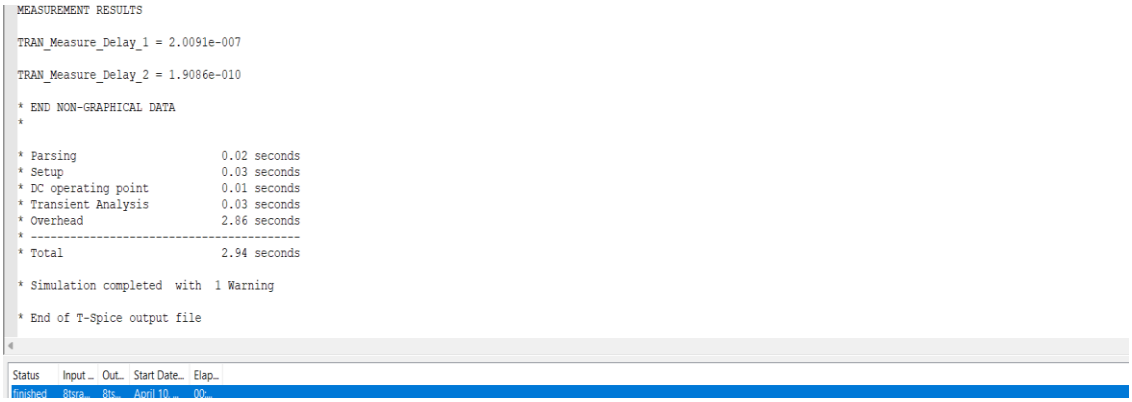

Fig.10: Delay Results of a 8T SRAM Cell

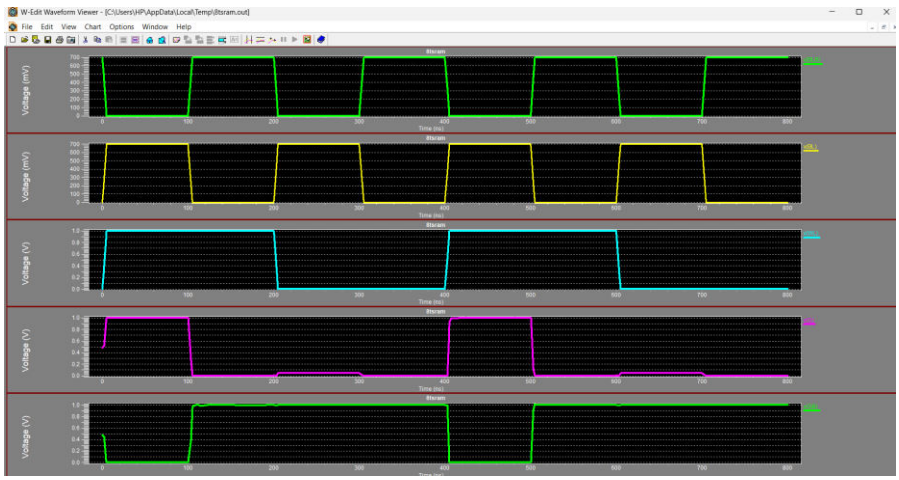

Fig.11: Simulation Results of a 8T SRAM Cell

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9T SRAM Cell Results

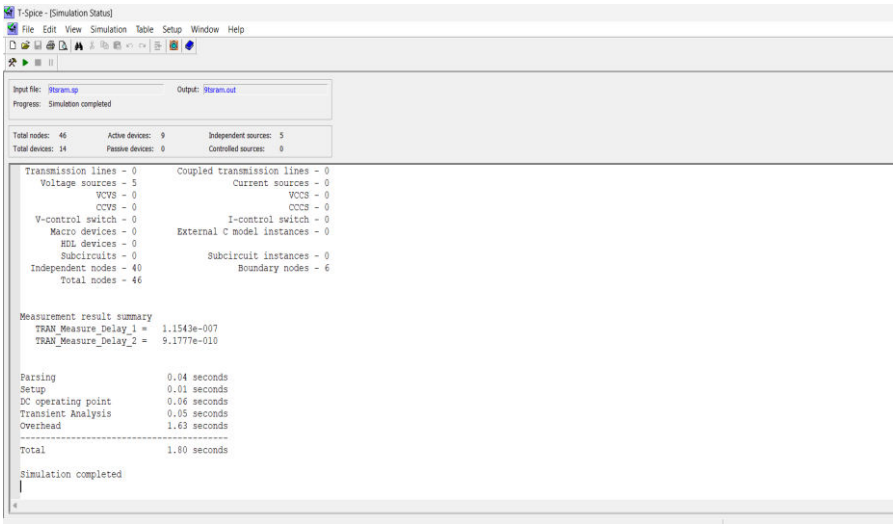

Fig.12: Power consumption results of 9T SRAM Cell

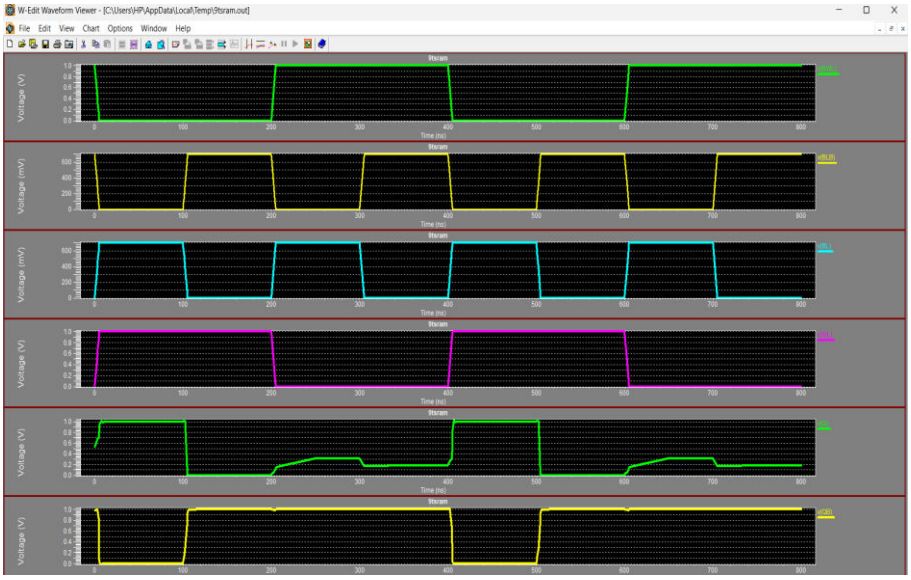

Fig.13: Simulation Results of 9T SRAM Cell

IV. CONCLUSION

The conclusion of the performance evaluation and comparison of 4T, 6T, 7T, 8T, and 9T SRAM at the 22nm technology node provides valuable insights into the characteristics and suitability of each SRAM cell design. the choice of SRAM cell design should be based on a thorough understanding of the application's requirements and trade-offs. While lower-transistor-count designs like the 4T and 6T SRAM cells may offer advantages in terms of area and speed, higher-transistor-count designs like the 9T SRAM cell provide enhanced stability and reliability, albeit at the cost of increased power consumption and area. Future research may focus on further optimizing SRAM cell designs to achieve a balance between performance, power efficiency, and area occupancy in advanced technology nodes.

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