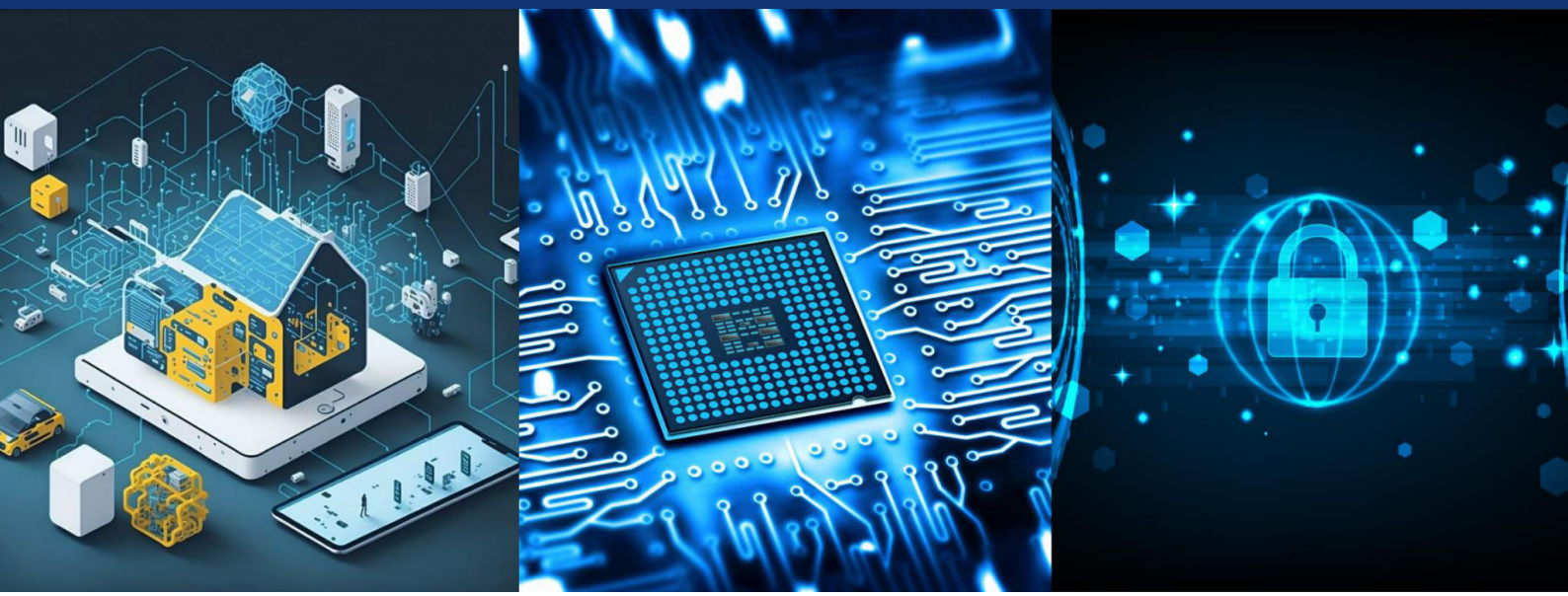
IJIRCCE

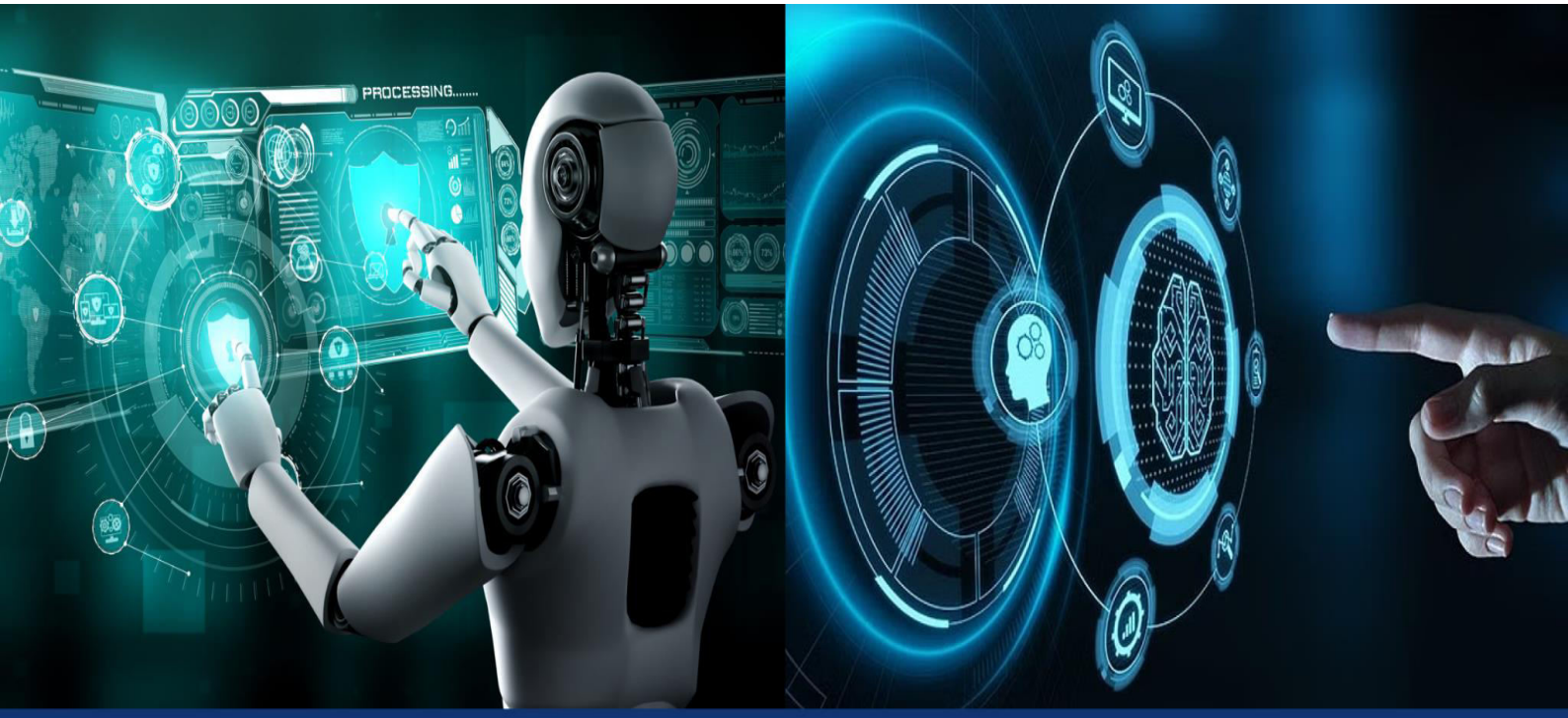
ISSN(O): 2320-9801

ISSN(P): 2320-9798



International Journal of Innovative Research in Computer and Communication Engineering

(A Monthly, Peer Reviewed, Refereed, Scholarly Indexed, Open Access Journal)



Impact Factor: 8.771

Volume 13, Issue 5, May 2025

© 2025 IJIRCCE | Volume 13, Issue 5, May 2025| DOI:10.15680/IJIRCCE.2025.1305082

www.ijircce.com | e-ISSN: 2320-9801, p-ISSN: 2320-9798| Impact Factor: 8.771| ESTD Year: 2013|

International Journal of Innovative Research in Computer and Communication Engineering (IJIRCCE)

(A Monthly, Peer Reviewed, Refereed, Scholarly Indexed, Open Access Journal)

Generative AI for Analog Integrated Circuit Design

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ABSTRACT: Analog Integrated Circuit (IC) design is a highly specialized and iterative process that demands extensive expertise and considerable development time. Traditional design methodologies rely heavily on manual adjustments and domain-specific heuristics, often limiting the pace of innovation and exploration. With the advent of Generative Artificial Intelligence (AI), there is a promising opportunity to revolutionize analog IC design by automating topology generation, parameter optimization, and performance enhancement. This paper presents a comprehensive exploration of generative AI techniques—such as Generative Adversarial Networks (GANs), Variational Autoencoders (VAEs), and Reinforcement Learning (RL)—and their application in analog IC synthesis. By learning from existing design libraries and performance datasets, these models can propose novel and efficient circuit architectures while addressing multi-objective design constraints like power, area, noise, and linearity. The integration of generative AI into analog IC workflows can significantly reduce design cycles, improve design quality, and expand the creative boundaries of circuit engineering. This work highlights current research trends, challenges, and the transformative potential of generative AI in shaping the future of analog IC design.

KEYWORDS: Analog Integrated Circuit Design, Generative AI, Circuit Topology Synthesis, Design Space Exploration.

I. INTRODUCTION

The increasing demand for high-performance, compact, and energy-efficient electronic systems has intensified the complexity of analog integrated circuit (IC) design. Unlike digital circuits, which benefit from standardized design methodologies and robust automation tools, analog IC design continues to rely heavily on manual expertise, iterative optimization, and domain-specific heuristics. The design of analog circuits involves addressing multiple conflicting objectives such as gain, bandwidth, power consumption, linearity, noise, and area efficiency. The intrinsic non-linear behaviour of analog components, coupled with susceptibility to process variations, makes the design space highly non-convex and difficult to navigate. Consequently, analog IC design remains a labor-intensive, time-consuming, and expertise-driven task that often limits the pace of innovation and scalability. The growing complexity and increasing performance requirements of analog systems in applications such as wireless communication, automotive electronics, biomedical devices, and Internet of Things (IoT) call for new, intelligent, and automated approaches to analog IC design. Generative Artificial Intelligence (AI) has recently emerged as a promising solution to address the challenges inherent in analog IC design. Generative AI refers to a class of machine learning models capable of creating new data instances that resemble a given dataset. Techniques such as Generative Adversarial Networks (GANs), Variational Auto encoders (VAEs), and Reinforcement Learning (RL) have shown remarkable success in fields like image generation, natural language processing, and drug discovery. These models can learn the underlying patterns and relationships within large datasets and subsequently generate novel and high-quality content. In the context of analog IC design, generative AI holds the potential to automate topology generation, parameter optimization, and performance enhancement by learning from existing circuit designs and simulation data. By exploring vast, high-dimensional, and non-linear design spaces, generative AI models can identify innovative solutions and optimal trade-offs that traditional heuristic or rule-based approaches might overlook.

The application of Generative AI in analog IC design introduces several advantages. First, it significantly reduces the design cycle by automating the traditionally manual and iterative processes of topology selection and device sizing. This enables rapid prototyping and accelerates the overall product development timeline. Second, generative AI models excel in multi-objective optimization, effectively managing trade-offs among conflicting performance metrics such as power, area, and linearity. This capability is particularly valuable in analog IC design, where achieving optimal performance across multiple objectives is a constant challenge. Third, generative AI facilitates enhanced design space exploration, uncovering unconventional and innovative circuit architectures that might be difficult for human designers

to conceive. Furthermore, by integrating data-driven decision-making into the design workflow, generative AI improves design robustness against process, voltage, and temperature variations, ultimately resulting in higher-quality and more reliable analog ICs. Several generative AI techniques have been adapted for use in analog IC design. Generative Adversarial Networks (GANs) consist of two neural networks: a generator and a discriminator. The generator creates new circuit designs, while the discriminator evaluates their feasibility and performance. Through this adversarial process, the generator progressively improves its design proposals. GANs have shown promise in tasks such as circuit topology generation and layout synthesis. Variational Autoencoders (VAEs), on the other hand, learn a probabilistic latent representation of circuit designs, enabling the generation of new designs by sampling from this latent space.

VAEs are well-suited for performance-driven design generation, data augmentation, and topology optimization. Reinforcement Learning (RL) involves training an agent to interact with the design environment by selecting actions such as choosing topologies or adjusting parameters. The agent receives feedback in the form of rewards based on the performance of the resulting design and learns an optimal policy for navigating the design space. RL has proven effective for multi-objective optimization, adaptive design strategies, and layout optimization. The motivation behind exploring generative AI for analog IC design stems from the pressing need for scalable, automated, and intelligent design methodologies. As the complexity of analog systems continues to grow, traditional design approaches struggle to keep pace with market demands for faster, smaller, and more power-efficient devices. Generative AI offers a means to not only automate existing design processes but also to discover entirely new design paradigms that push the boundaries of conventional analog circuit design. By leveraging the vast amounts of data generated from circuit simulations, characterization, and historical design libraries, generative AI models can learn intricate design principles and generate novel circuits that meet specific performance criteria.

The scope of this paper encompasses a comprehensive exploration of the application of generative AI techniques in analog IC design. It begins with a discussion of the inherent challenges in analog design and the limitations of conventional methodologies. This is followed by an in-depth examination of various generative AI models, including GANs, VAEs, and RL, highlighting their underlying principles, advantages, and adaptation to circuit design problems. The paper then reviews recent research efforts and case studies that demonstrate the practical application of generative AI in tasks such as topology synthesis, device sizing, and performance optimization. Additionally, the paper identifies existing research gaps, practical limitations, and opportunities for future advancements in this emerging field. In summary, the integration of generative AI into analog IC design workflows presents a transformative opportunity to enhance productivity, foster innovation, and democratize access to high-quality analog circuit designs. By automating labor-intensive tasks, optimizing complex multi-objective problems, and expanding the boundaries of design space exploration, generative AI has the potential to revolutionize the way analog ICs are conceived, developed, and deployed. As the field continues to evolve, on going research and collaboration between the AI and electronic design automation communities will be essential to fully realize the benefits of this promising technology.

II. LITERATURE SURVEY

[1]. Chen et al. (2022) – "Generative adversarial networks for analog IC layout synthesis". The address one of the longstanding bottlenecks in analog IC design — the laborious and iterative nature of manual layout generation. In their paper, they propose a GAN-based framework tailored for analog layout synthesis, which automates the generation of layout geometries while preserving critical design rules and matching constraints. The generator network is trained to produce layout patterns resembling those from expert-designed layouts, while the discriminator evaluates the realism and compliance of the generated layouts with layout-versus-schematic (LVS) standards. The study demonstrates that by learning from a dataset of annotated layout designs, the GAN model can effectively capture complex spatial relationships, symmetry requirements, and placement-routing strategies inherent to analog layouts. The framework also incorporates a layout constraint embedding mechanism, enabling the model to adhere to specific design rule constraints such as spacing, alignment, and symmetry during generation.

[2]. Liu et al. present a comprehensive review covering the recent advancements in applying machine learning and generative AI models for analog IC design tasks. The survey spans techniques such as Variational Autoencoders (VAEs), Generative Adversarial Networks (GANs), and diffusion models, focusing on their use in performance prediction, topology generation, device sizing, and layout automation. The authors highlight the strengths and limitations of each approach while comparing AI-based workflows with conventional Electronic Design Automation

(EDA) tools. The study also discusses challenges like data scarcity, model interpretability, and integrating AI tools within existing analog design environments. Their work serves as a valuable resource for identifying emerging trends and future directions in AI-driven analog IC automation.

[3]. Zhang & Roychowdhury (2022) – "Generative models for topology synthesis of analog circuits". In this paper, Zhang and Roychowdhury propose a framework based on Variational Autoencoders (VAEs) for the automated generation of valid analog circuit topologies. The authors show how the latent space learned by the VAE can be leveraged for controlled exploration of circuit topologies, allowing designers to interpolate between existing designs or extrapolate novel structures. Their method enables the generation of performance-optimized and specification-compliant designs with minimal human intervention. The study also emphasizes the importance of ensuring connectivity and functionality constraints within the generative model, which is crucial for producing electrically valid topologies. Experimental validation on analog building blocks like amplifiers and current mirrors confirms the efficiency of their approach in rapidly generating optimized, diverse design candidates.

[4]. Kandasamy et al. investigate the integration of Neural Architecture Search (NAS) techniques with generative AI models to automate analog circuit design workflows. Their review covers various NAS strategies adapted for analog design, detailing how these methods autonomously discover optimal circuit configurations and performance trade-offs. The authors highlight the synergy between NAS and generative models like GANs and VAEs in navigating large, high-dimensional design spaces efficiently. Additionally, the paper discusses the benefits of AI-guided search algorithms in reducing design cycle times, enhancing design space exploration, and improving overall circuit performance. The study concludes by identifying potential research gaps in combining NAS with reinforcement learning and differentiable simulation frameworks for analog IC applications.

[5] Noori Zadeh & Elamien (2025) – "Generative AI for Analog Integrated Circuit Design: Methodologies and Applications". This systematic review discusses recent contributions over the last five years, highlighting methods that address data scarcity, topology exploration, process-voltage-temperature (PVT) variations, and layout parasitics. The authors provide a methodological review of state-of-the-art machine learning approaches, including graph neural networks (GNNs), large language models (LLMs), and variational autoencoders (VAEs), applied to analog circuit sizing tasks. They conclude that future research could focus on few-shot learning with domain-adoption training of generative AI methods to simplify design tasks such as human-tool interaction or guided design space exploration.

III. ANALOG INTEGRATED CIRCUIT DESIGN: METHODOLOGY

The methodology for designing analogy integrated circuits (ICs) encompasses a series of well-established steps, from the initial concept to the final physical design. However, the conventional process is often manual and highly iterative, requiring extensive expertise and time to ensure a design meets performance requirements. With the increasing complexity of circuits and demand for faster development times, modern approaches integrate advanced methodologies and tools, including simulation, optimization, and layout design, while considering constraints like power, area, and performance metrics.

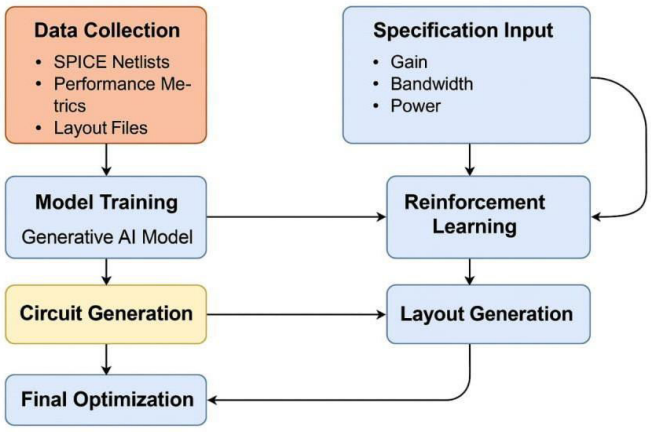

Fig 1: System Architecture of Generative AI for Analog Integrated Circuit Design.

© 2025 IJIRCCE | Volume 13, Issue 5, May 2025| DOI:10.15680/IJIRCCE.2025.1305082

www.ijircce.com | e-ISSN: 2320-9801, p-ISSN: 2320-9798| Impact Factor: 8.771| ESTD Year: 2013|

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The methodology for implementing generative artificial intelligence in analogy integrated circuit (IC) design is systematically outlined in the given workflow diagram. The process begins with **data collection**, where a comprehensive dataset consisting of SPICE netlists, performance metrics, and layout files is gathered. These datasets form the foundation for training the AI models, as they contain crucial information about existing circuit designs, their corresponding performance specifications, and physical layout details. Alongside this, **specification input** is provided by designers, outlining the desired operational parameters such as gain, bandwidth, and power consumption. These specifications serve as target objectives for the AI system to meet while generating new circuit designs. Following data preparation, **model training** is carried out using advanced generative AI models such as Generative Adversarial Networks (GANs), Variational Auto encoders (VAEs), or diffusion models. These models are trained to learn the complex relationship between circuit topologies and their corresponding performance outcomes. Once trained, the AI model enters a **reinforcement learning** phase, where it iteratively improves its generation capabilities by receiving feedback from simulated circuit performances. This learning loop ensures that the AI-generated designs progressively align better with the desired specifications.

The next stage involves circuit generation, where the trained generative model produces candidate circuit topologies based on the provided specifications. These generated designs are then processed through layout generation tools, which automatically create the physical layouts for the circuits while adhering to design rule constraints and ensuring layout-versus-schematic (LVS) compliance. The final stage of the workflow is final optimization, where post-layout simulations and adjustments are performed to fine-tune the design. This step ensures that the final circuits not only function correctly but also meet high-performance standards and are robust against variations in manufacturing processes. Throughout the workflow, feedback loops from specification input to reinforcement learning and from final optimization back to earlier stages enable continuous refinement and improvement of the circuit generation process. This end-to-end methodology greatly accelerates the analogy IC design cycle, reduces manual efforts, and promotes the creation of innovative, high-performance designs.

IV. ANALOG INTEGRATED CIRCUIT DESIGN: CHALLENGES AND LIMITATIONS

Analog integrated circuit (IC) design faces several challenges due to its inherent complexity and the limitations of traditional methods. One of the main obstacles is the vast design space, where even small changes in circuit parameters can significantly affect performance. This makes it difficult to explore all possible configurations efficiently. Analog design also requires balancing multiple conflicting performance objectives such as power consumption, gain, linearity, and noise immunity. Traditional design methods struggle to optimize these conflicting goals simultaneously, making the process time-consuming and error-prone.

Additionally, analogy circuits are highly sensitive to manufacturing process variations, which can cause significant performance degradation. The non-linear behaviour of analogy components further complicates the design and simulation processes. Ensuring compliance with design rules, such as proper spacing and routing, is another major challenge. These rules are critical for manufacturability but are difficult to enforce manually, especially as circuits become more complex. Moreover, the integration of analogy and digital components in a modern system-on-chip (SoC) design introduces additional difficulties, including managing noise and interference between the two domains. Another limitation is the lack of standardized and automated tools for analogy IC design. While digital design benefits from highly automated Electronic Design Automation (EDA) tools, analogy design still requires considerable manual intervention, particularly for layout and optimization. This lack of automation increases dependence on the designer's **expertise**, resulting in **slower development times** and **inconsistent results**. As the demands for high-performance analogy circuits grow, addressing these challenges through **automation** and advanced techniques, such as **generative AI**, becomes increasingly important for improving **efficiency** and **accuracy** in analogy IC design.

V. GENERATIVE AI TECHNIQUES FOR ANALOG IC DESIGN

The integration of generative artificial intelligence techniques into analogy integrated circuit (IC) design has introduced novel possibilities for automating complex and traditionally manual design tasks. Among the prominent AI techniques, Generative Adversarial Networks (GANs) have gained significant attention for their ability to generate realistic and high-quality circuit layouts. GANs consist of two competing neural networks—a generator and a discriminator—that work in tandem to improve the quality of generated designs. In the context of analogy IC design, GANs can learn intricate layout patterns and constraints from existing datasets, thereby reducing manual layout efforts and ensuring

design rule compliance and layout-versus-schematic (LVS) accuracy. By training on a wide range of existing layouts and their associated performance metrics, GANs are capable of proposing innovative and performance-optimized circuit configurations.

Another widely adopted technique is the Variational Autoencoder (VAE), which focuses on learning compact latent representations of circuit topologies. VAEs map input data into a continuous latent space, allowing for smooth interpolation and controlled exploration of new circuit configurations. This capability enables designers to rapidly generate a variety of feasible topologies by sampling from the latent space and adjusting parameters to meet specific performance goals such as gain, linearity, power consumption, and area. The use of VAEs is particularly advantageous in topology synthesis, where the exploration of multiple design alternatives is essential to optimize for multi-objective constraints. Reinforcement learning (RL) is also proving to be a valuable tool in analogy IC design automation. In this technique, an AI agent iteratively interacts with a simulated environment, receiving feedback based on the performance of generated circuits. The agent updates its policy to maximize rewards, which are typically linked to how well the generated designs satisfy the desired specifications. RL is highly effective for tasks involving sequential decision-making, such as component placement, topology optimization, and performance tuning, where each decision impacts subsequent design outcomes. Additionally, diffusion models—a recent advancement in generative modelling—are being explored for their ability to progressively refine noisy initial designs into high-quality, specification-compliant circuits.

These models operate by simulating a denoising process that iteratively improves the generated design, making them well-suited for navigating complex and high-dimensional design spaces typical in analog IC design. By combining these generative AI techniques within a unified design framework, it becomes possible to address several longstanding challenges in analog IC design, including limited automation, lengthy design cycles, and the difficulty of multi-objective optimization. These models not only accelerate design processes but also foster innovation by uncovering novel topologies and layouts that might not emerge through conventional manual design practices. As the field continues to evolve, the integration of these AI-driven techniques promises to redefine the future of analogy IC design automation.

VI. APPLICATIONS OF GENERATIVE AI IN ANALOG IC DESIGN

The application of generative artificial intelligence in analog integrated circuit (IC) design is transforming several critical stages of the design workflow, addressing longstanding challenges related to manual effort, design space exploration, and optimization under multi-objective constraints. One of the primary applications is in circuit topology generation, where generative models like GANs and VAEs automatically create novel and functionally viable analog circuit topologies based on specified performance targets such as gain, bandwidth, power consumption, and linearity. This capability enables designers to explore a broader and more diverse set of design alternatives in a significantly shorter time, leading to more efficient and innovative circuit solutions.

Another important application lies in layout automation, where generative AI models, particularly GAN-based frameworks, have demonstrated impressive capabilities in generating high-quality physical layouts while ensuring design rule compliance and layout-versus-schematic (LVS) accuracy. These AI-driven layout generators can learn from large collections of existing layouts, capturing intricate patterns and constraints that are traditionally managed by experienced layout engineers. As a result, they can produce layouts that are not only functionally correct but also optimized for performance metrics such as area, parasitic capacitance, and yield.

Generative AI also finds application in performance prediction and optimization. By learning the relationship between circuit topologies and their performance outcomes, AI models can quickly estimate the performance of newly generated designs without exhaustive SPICE simulations. This rapid feedback enables designers to identify promising candidates early in the design cycle and iteratively refine them using reinforcement learning loops or optimization algorithms, ultimately leading to better-performing designs within reduced timelines.

Furthermore, generative AI models are increasingly applied in multi-objective optimization, a complex and resource-intensive task in analog IC design. By simultaneously considering trade-offs between various performance metrics, these models can generate designs that achieve balanced performance across conflicting objectives, such as minimizing power consumption while maximizing gain and bandwidth. The ability of generative models to handle such multi-

dimensional optimization problems effectively accelerates the design process and enhances the final product's competitiveness. Lastly, generative AI is contributing to design migration and adaptation, where existing circuit designs are automatically adapted to new process nodes, supply voltages, or performance requirements. AI-driven approaches can quickly reconfigure topologies and layout structures to accommodate changes in manufacturing technology, reducing the time and effort traditionally required for such tasks. Overall, the integration of generative AI into these diverse applications signifies a major advancement in analogy IC design automation, offering new possibilities for improving efficiency, innovation, and design quality in the semiconductor industry.

VII. CONCLUSION AND FUTURE WORK

Generative artificial intelligence (AI) has introduced transformative possibilities in analogy integrated circuit (IC) design by addressing long-standing challenges such as manual topology generation, complex optimization, and lengthy design cycles. This paper discussed how generative models like GANs, VAEs, and reinforcement learning can automate tasks ranging from circuit topology synthesis to layout generation and performance optimization. These AI-driven techniques not only accelerate design workflows but also enhance performance metrics by exploring a wider design space. Moving forward, future work should focus on developing larger, high-quality analog design datasets, improving model interpretability and robustness, and integrating AI tools seamlessly with existing EDA platforms. Additionally, leveraging AI for design migration to newer technology nodes and further advancing multi-objective optimization techniques will help unlock the full potential of generative AI in analogy IC design.

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