IJIRCCE

e-ISSN: 2320-9801 | p-ISSN: 2320-9798

INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH

IN COMPUTER & COMMUNICATION ENGINEERING

Volume 11, Issue 5, May 2023

INTERNATIONAL STANDARD SERIAL NUMBER INDIA

Impact Factor: 8.379

International Journal of Innovative Research in Computer and Communication Engineering

| e-ISSN: 2320-9801, p-ISSN: 2320-9798| www.ijircce.com | |Impact Factor: 8.379 |

|| Volume 11, Issue 5, May 2023 ||

| DOI: 10.15680/IJIRCCE.2023.1105019 |

Design and VLSI Implementation of Low Power Sense Amplifier

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ABSTRACT: The sensing amplifier circuit is one of the memory's most important component. It is used to gain access to the information stored in the bit cell during the read cycle. The sense amplifier brings the minute voltage disparities between bit lines up to full swing. Due to reduced sense amplifier detection latency and power consumption, memory performance is improved. Its execution has an impact on memory's access time and power distribution. The majority of memory-related operations are read-only, which dramatically lowers the total amount of power that the memory dissipates.Sense amplifiers scatter a big quantity of short out power rather than the dynamic power that the cell propagates, which also saves a lot of power. The market for reliable, fast-CMOS, low-power, simple VLSI circuits is expanding dramatically. The drive for innovation that arises from shrinking the base component size to minimize the chip zone is what led to this evolution. It will be feasible to put more circuit segments onto a single chip and lower the cost by shrinking the transistor. Furthermore, smaller shapes frequently have lower parasitic capacitances, which indicates higher working speeds and less control utilization. Sense amplifiers are essential for the reliability and efficiency of memory circuits. The PMOS biased sense amplifier and latch sense amplifier in the proposed circuit has very high output impedances, minimal power dissipation, and a low sense latency. The recommended circuits accomplish the same objectives as traditional circuits while using less power and having less sensing delay. The recommended sense amplifiers' total performance has been simulated and evaluated using Cadence Virtuoso and the gpdk 180 nm, gpdk90 nm, and gpdk45 nm library parameters.

KEYWORDS*:* Sense amplifier, Delay;

I. INTRODUCTION

A sense amplifier is a crucial component in many digital circuits, especially in memory devices such as DRAMs (Dynamic Random-Access Memories) and SRAMs (Static Random-Access Memories). The main function of a sense amplifier is to detect and amplify small signals from memory cells, which represent the stored data [1]. The amplified signals are then used to determine the logical state of the memory cells, i.e., whether they are storing a ”0” or a ”1” [10]. The basic circuitry of a sense amplifier consists of a differential amplifier and a latch. The differential amplifier compares the voltage levels of two input signals, which represent the stored data in a memory cell. The output of the differential amplifier is then fed to a latch, which stores the amplified signal and provides the output to the memory circuit. There are several types of sense amplifiers used in memory circuits, such as single-ended sense amplifiers, differential sense amplifiers, and folded bit-line sense amplifiers. Single-ended sense amplifiers use a single-ended input signal, while differential sense amplifiers use a differential input signal. Folded bit-line sense amplifiers are a variation of differential sense amplifiers, where the bit-lines are folded back on themselves to reduce the chip area. The operation of a sense amplifier can be divided into two stages: pre-charge and sense. During the pre-charge stage, the bit-lines in the memory

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circuit are charged to a reference voltage level. This ensures that the output of the sense amplifier is within the valid range of logic levels. During the sense stage, the stored data in a memory cell is read by activating the corresponding word-line and enabling the sense amplifier. The sense amplifier then detects and amplifies the small signal from the memory cell, and provides the amplified output to the memory circuit. The design of a sense amplifier depends on several factors, such as the memory cell size, the operating frequency, and the power consumption. One of the key considerations in the design of a sense amplifier is its speed, as it determines the read access time of the memory circuit. Another important consideration is the noise margin of the sense amplifier, which determines the minimum signal level that can be detected and amplified. The noise margin is affected by various factors such as the device mismatch, parasitic capacitance, and the input offset voltage. The power consumption of a sense amplifier is also an important factor, as it affects the overall power consumption of the memory circuit. Various techniques such as voltage scaling, current scaling, and adaptive biasing are used to reduce the power consumption of sense amplifiers. In conclusion, sense amplifiers are an essential component of memory circuits, and their design and operation play a critical role in the overall performance and power consumption of memory devices. The design of sense amplifiers involves a trade-off between speed, noise margin, and power consumption, and various techniques are used to optimize these parameters. With the increasing demand for high-speed and low-power memory devices, the design and optimization of sense amplifiers will continue to be an active research area in the field of digital circuit design.

II. THEORETICALBACKGROUND

In digital circuits, a sense amplifier is used to amplify the voltage difference between two nodes. In CMOS technology, a P-MOS biased sense amplifier is commonly used in memory circuits to amplify the small voltage difference between the bit-line and the reference voltage. The basic circuit of a P-MOS biased sense amplifier consists of a P-MOS transistor and an N-MOS transistor, connected in series between the bit-line and the power supply. The gate of the P-MOS transistor is connected to the reference voltage, while the gate of the N-MOS transistor is connected to the complement of the reference voltage.When the bit-line voltage is lower than the reference voltage, the P-MOS transistor is turned off and the N-MOS transistor is turned on, creating a low resistance path between the bit-line and ground. This causes the voltage on the bit-line to be pulled down to ground. When the bit-line voltage is higher than the reference voltage, the P-MOS transistor is turned on and the N-MOS transistor is turned off, creating a high resistance path between the bit-line and power supply. This allows the bit-line voltage to be amplified to a higher voltage.The P-MOS biased sense amplifier is advantageous because it has a high voltage gain, low power consumption, and a simple structure. It is also relatively immune to process variations, which can cause differences in the threshold voltages of the transistors. However, it is limited in its speed due to the inherent capacitance of the bit-line and the need to charge and discharge it during the amplification process [1].

A latched sense amplifier is another type of sense amplifier commonly used in CMOS technology. It is a type of regenerative sense amplifier that uses positive feedback to amplify the small voltage difference between the bit-line and the reference voltage.The basic circuit of a latched sense amplifier consists of a cross-coupled pair of inverters, two access transistors, and a feedback transistor. The access transistors are connected between the bit-line and the input of each inverter, while the feedback transistor is connected between the output of one inverter and the input of the other inverter. When the bit-line voltage is lower than the reference voltage, the access transistors are turned off and the cross-coupled inverters maintain their previous state. This allows the sense amplifier to hold its output, even after the input voltage is removed. When the bit-line voltage is higher than the reference voltage, the access transistors are turned on, and the voltage difference is amplified through positive feedback, causing the sense amplifier output to change state.The latched sense amplifier has a number of advantages, including high speed, high voltage gain, and good noise immunity. However, it is also more complex than other types of sense amplifiers, and requires careful design and optimization to achieve the desired performance [10].

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III. DESIGN AND IMPLEMENTATION

3.1 Design for Implementation of Sense Amplifier

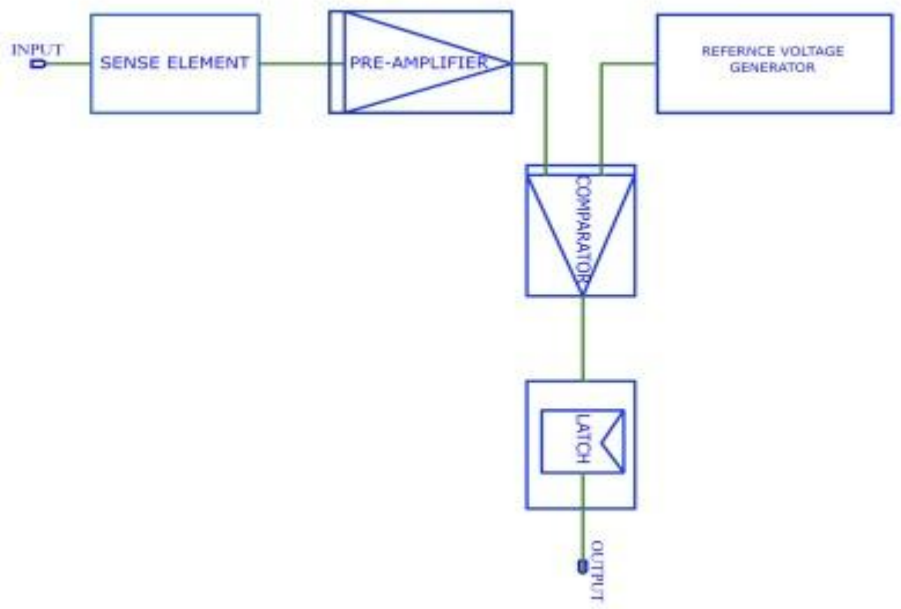

Figure3.1:Blockdiagramof Sense Amplifier

1. **Input Voltage**: Input voltage is the small voltage which needs to be amplified. It is the output voltage from the magnetic sensors of the memory or from any other sensor. This voltage cannot be represented as a logic high voltage for decision making or for any other application.

2. **Sense amplifier**: Sense element is basically an electronic circuit which produces an output voltage which is proportional to the input voltage. This circuit will buffer out the input signal which basically reduces the noise present in the input to the sense element.

3. **Pre-Amplifier**: The output of the sense element is fed to the pre amplifier which amplifies the input voltage to the desired voltage. When a memory read operation takes place there will be a small voltage difference between bit line and bit line bar which will be sensed by the sense element of the sense amplifier circuitry, then this voltage will be amplified to a desired voltage level.

4. **Reference voltage generator**: This stage contains an electronic circuit to generate voltage of desired level of amplitude. This voltage is used as reference voltage for the amplified voltage from the pre-amplifier.

5. **Comparator**: This stage contains a comparator circuit. Comparator circuit basically contains two inputs namely reference voltage and input voltage or the voltage which needs to be compared with the reference voltage. After comparing the voltage with the reference voltage, it will generate digital voltage.

6. **Latch**: A latch or a Flip flop is a 1-bit memory storing element. The latch is used to store the digital output from the comparator as long as sense amplifier is not reset to initial condition or next cycle output from the comparator arrives.

7. **Output:** Output stage is the final stage of sense amplifier which will provide the amplified output of small sensed input voltage. The output voltage is noise free and can be utilized for decision making in memory read operation.

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3.4 Schematic

3.4.1 PMOS biased sense amplifier**:**

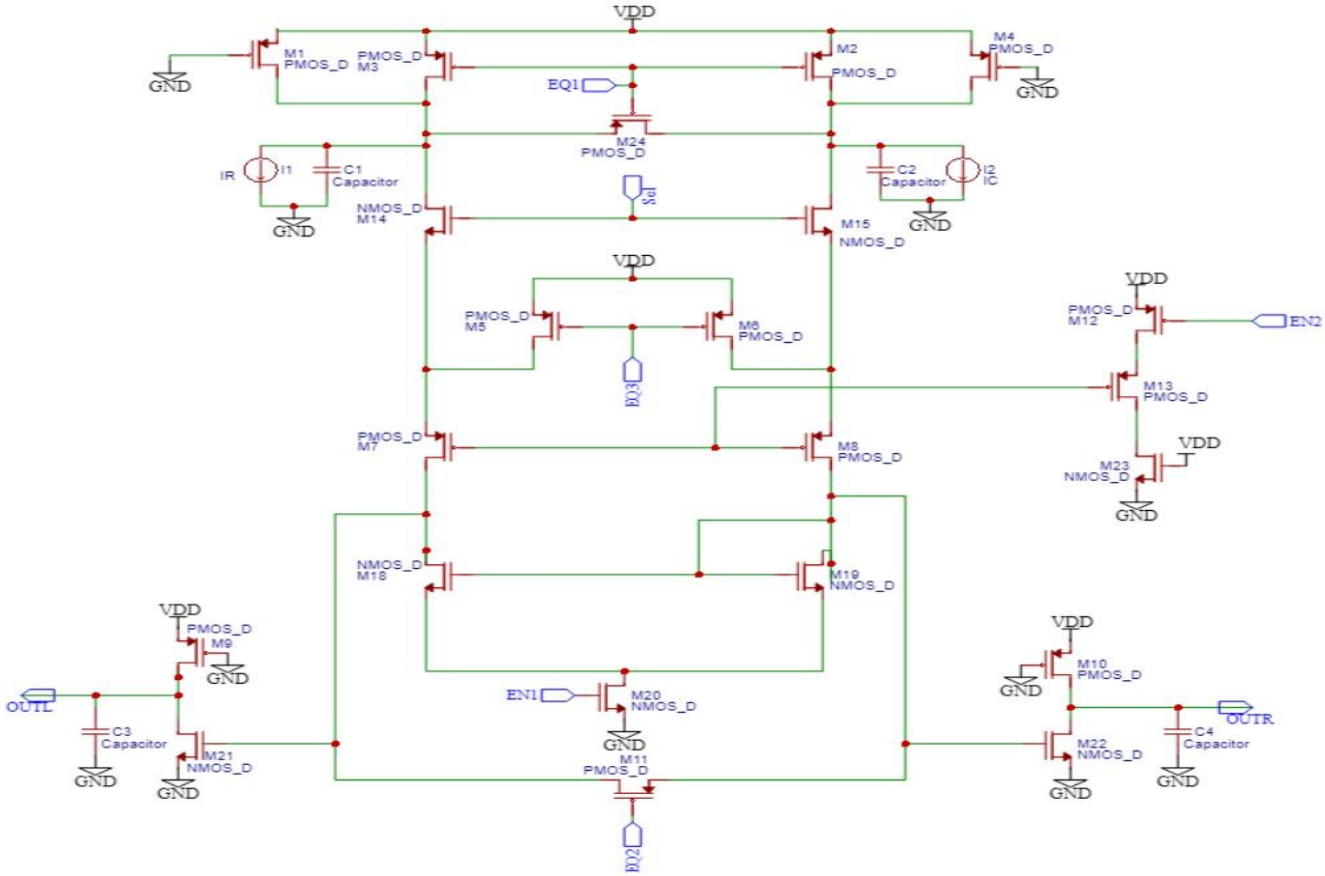

Figure.3PMOS biased sense amplifier[1]

This circuit consists of CMOS (Complementary metal oxide semiconductor) transistors. The sense amplifiers process is divided into two steps: detecting the signal before charging it, and sensing the signal after it has been amplified by the circuit.It consists of PMOS (P channel metal oxide semiconductor) transistor in the pull up network. Pull up network or pull up load is the component of the circuit which is directly connected to the power supply. In this circuit PMOS M1, M2, M3, M4 are the pull up transistors. The transistor M24, M3 M2 gate terminal are shorted and connected to the "EQ1" (EQ stand for Equalization terminal). Equalization pins are used to equalize the voltage on the pair of sense lines. Equalizing the sense line will help sensing the voltage difference between the bit line and bit line bar. The current source Ir and Ic are used to maintain difference in current flowing through bit line bit line bar. The current Ir is greater than the Ic which will make Ib-Id (Ib is the bit line current and Id is the difference current between Ir and Ic) to flow through the bit line and Ib to flow through bit line bar. "Sel" pin used to select which input to be amplified by the sense amplifier, which is connected to the shorted gate of M14 and M15 NMOS devices.M5 and M6 PMOS transistors will act as a pass transistor which are controlled by the "EQ3" which will maintain a constant voltage between the two drain terminals of the PMOS, this part of circuit is known as voltage bias generator. M7 and M8 PMOS are controlled by a voltage from a tiny circuit which in turn is controlled by the pin "EN2". EN stand for enable and controls which part of the circuit to be turned at a desired time. This will help to save the energy when the circuit is turned off by the enable pin. Transistor M16 and M17 gates are shorted and connected to drain of M16 transistor which will act as a current mirror circuit. Current mirror circuit is a circuit which forces the transistors to have the same current flowing through other. The output OUTL is considered across the shorted drain terminals of transistor M7 PMOS and M16 NMOS and output OUTR is considered

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across the shorted drain terminal of M8 PMOS and M17 NMOS transistor. The connection to the ground is controlled by terminal "EN1". Transistor M18 and M19 also performs the current mirror action. The output circuit consists of PMOS and NMOS which are in series.

3.4.2. Latched sense amplifier:

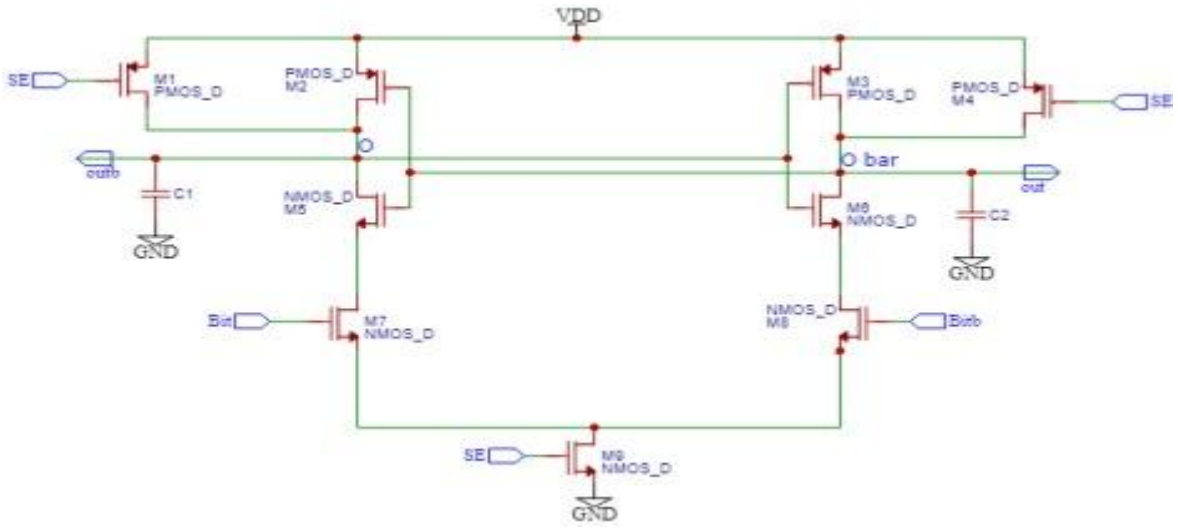

Figure 4 Latched sense amplifier[10]

This circuit is made up of the CMOS (Complementary metal oxide semiconductor) transistors. This circuit consists of four PMOS (P channel metal oxide semiconductor) transistor in pull up network. PMOS M1, M2, M3, M4 are in pull up network which will supply voltage through it to other part of the circuit depending on the gate control signal. PMOS M1 and M4 gate terminal are connected to the "SE" which is the select pin which will control which input to be amplified. PMOS M2 and NMOS M5 are connected in series and output is considered across shorted terminal of both transistor M2 and M5. Similarly, M3 and M6 are connected in series and output is considered across the shorted drain terminal of both transistors. The input to the sense amplifier is bit line and bit line bar are connected to the gate M7 and M8 which are in series with NMOS transistor M5 and M6 respectively. The select pin is also connected to the gate of M9 NMOS transistor which define a path to ground depending upon select line The bit line signal difference effects on the gate voltage of transistors MN1 and MN2. There is no current flow from bit lines to output nodes. When sensing signal SE is at logic 0 (GND), the output node is isolated to GND, and the precharge transistors MP3, MP4 charge output nodes to Vdd. Because the output nodes O and O are precharged to Vdd, the transistors MP1, MP2 are at cut-off region and MN4, MN5 are at saturation region. When the sensing signal SE changes to logic 1 (Vdd), MN3 is turned on and the node S is pulled down to GND level. Under this condition, MN1 and MN2 are workingas a common source differential amplifier. The voltage difference between Bit and Bit bar is transferred to the output nodes O and O bar by the common source differential amplifier. After a small voltage difference between O and O bar is generated, the crosscoupled amplifier which is constructed by MN4, MN5, MP1 and MP2 will finally amplify the voltage difference between O and O to a full swing voltage level. Therefore, we can sense and amplify the bit line signal without any current drifting from bit line to output node.

IV.RESULT AND DISCUSSION

During the process of implementation of sense amplifier, we have implemented a PMOS biased sense amplifier and a latch sense amplifier. The circuit mainly consists of CMOS devices to amplify the voltage which is sensed between the bit line and bit line bar. The circuit is constructed using the Cadence virtuoso analog design environment. The results are obtained using the ADEL tool inside the Virtuoso design environment. The timing analysis of the circuit is carried out using the transient analysis of the ADEL tool. Transient analysis will provide a graphical output of the selected input and output terminal of the circuit. When the designed circuit is simulated using the ADEL tool, we obtained an output waveform for output terminals.

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- Following images represents implementation of circuit and output in gpdk180

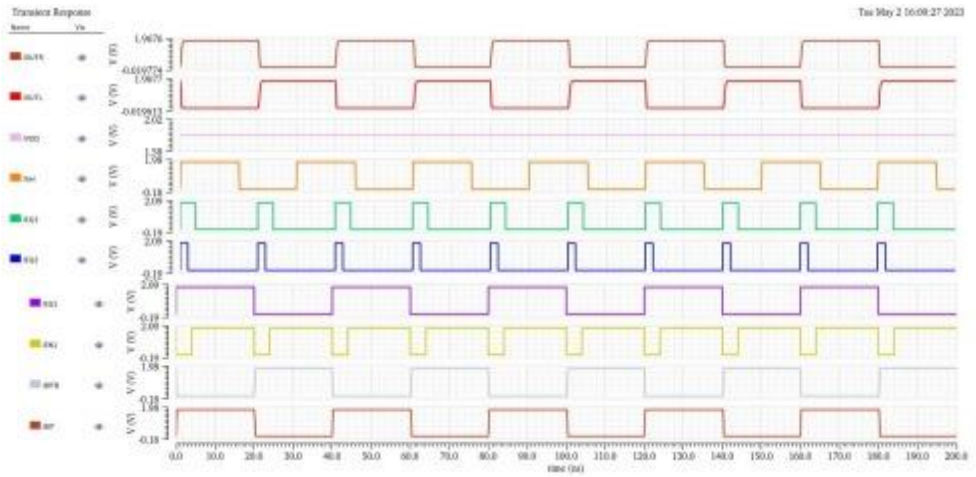

Figure 5: Output waveform of pmos biased sense amplifier using 180 technology

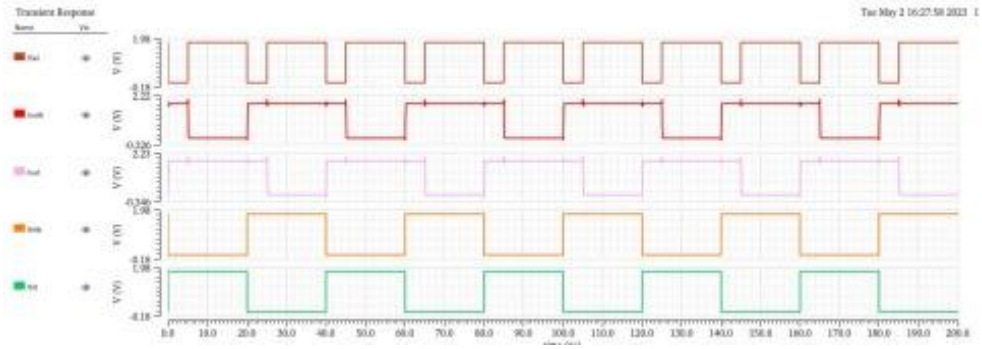

Figure 6: Output waveform of latched sense amplifier using 180 technology

- Following images represents implementation of circuit and output in gpdk90

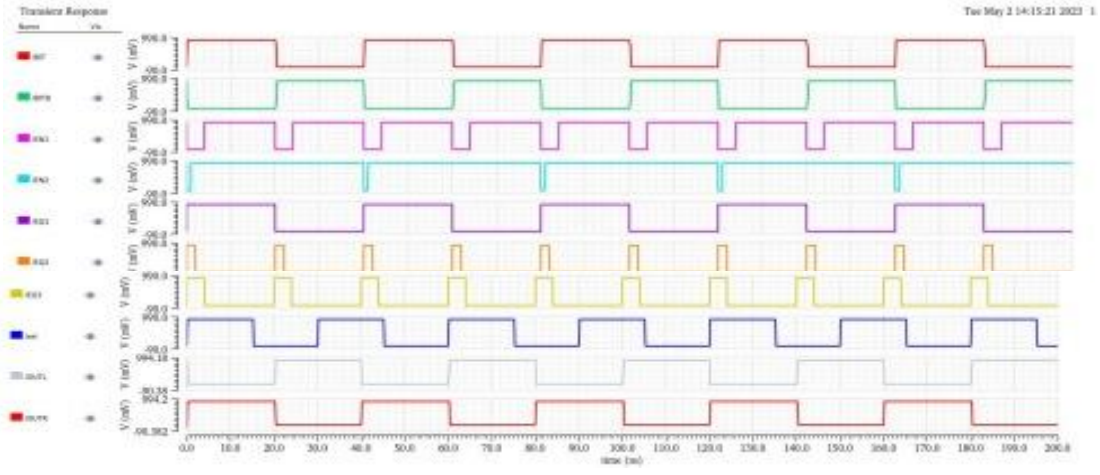

Figure 7: Output waveform of pmos biased sense amplifier using 90 technology

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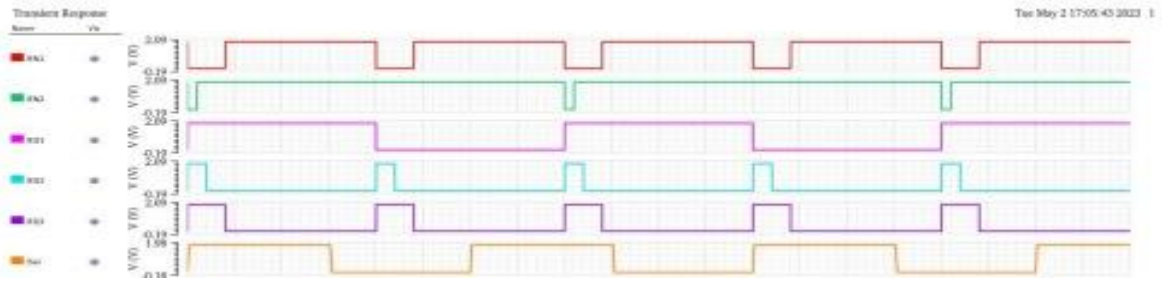

Figure 8: Output waveform of latched sense amplifier using 90 technology

- Following images represents implementation of circuit and output in gpdk45

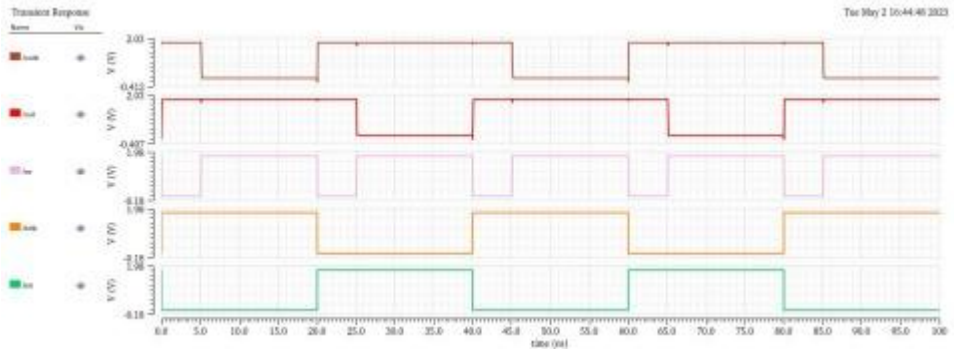

Figure 9: Output waveform of pmos biased sense amplifier using 45 technology

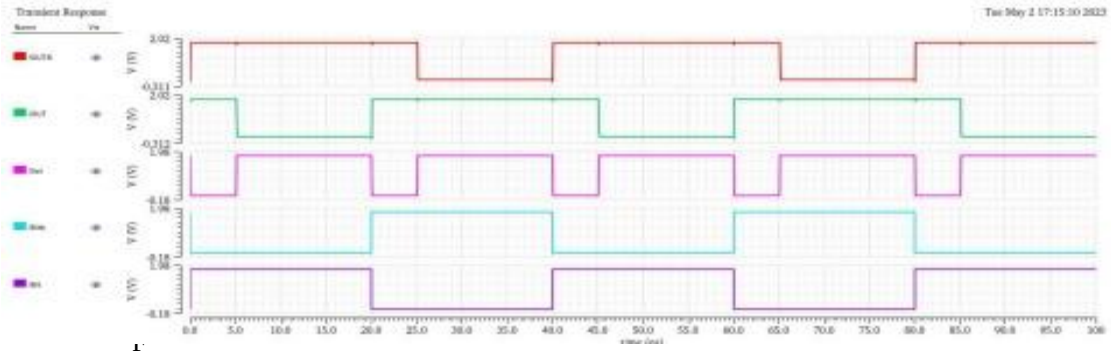

Figure 10: Output waveform of latched sense amplifier using 45 technology

IV. CONCLUSION

The goal of this project is to develop a sense amplifier circuit with less power consumption and less sensing delay. The proposed circuits are efficient memory read operation while maintaining less sensing delay and lowering the power consumption. All the circuits were constructed and verified the working using cadence virtuoso design environment. The PMOS biased sense amplifier transient analysis shows its dependency on the equalizer pin, select pin. These pins will

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help to maintain an equal amount of voltage in two complementary bit line. Equalizer pin will be active during the pre-charge state and charge both the bit line to equal voltage. During the read cycle SEL" pin will also affect the output voltage. The result shows that delay and power consumption of this circuit is minimal in gpdk45 technology. This proves the dependency of delay power consumption on transistor parameters such as channel length, width etc. The transient analysis of the Latch sense amplifier shows the dependency of output on" SEL" pin. When SEL pin is disabled, the circuit will be in pre charge state and when it is asserted to high value the circuit starts to amplify the voltage difference between bit and bit bar to a full swing voltage level. The delay of the circuit is minimal in gpdk45 technology due to smaller channel length. For the verification of circuit correctness, the input is provided as square wave with different pulse width and period to achieve different combination of input. The circuit provided the correct result for different input combinations.

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Impact Factor: 8.379

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ISSN INTERNATIONAL STANDARD SERIAL NUMBER INDIA

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