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A 6-Bit Full-360° Vector-Sum Phase Shifter Operating at 6–18 GHz with Low Error in 40-nm CMOS Technology

Dr. P. V. Murali Krishna[1], Goka Divya[2], Bushi Rajesh[3], Byri Rohini[4], Dronamraju Karthikeya[5]

Assistant Professor, Department of Electronics and Communication Engineering, GMR Institute of Technology, Rajam, A.P. India[1]

Students, Department of Electronics and Communication Engineering, GMR Institute of Technology, Rajam,

A.P. India[2-5]

ABSTRACT: A 6-bit full-360° vector-sum phase shifter that operates from 6 to 18 GHz has been developed using SMIC's 40-nm CMOS technology. The proposed design gets quite high precision with very low error, and hence is well-suited for the high-performance communication systems, radar, and phased array antennas. There is proper phase shifting with absolute accuracy through an innovative RC third-order IQ signal generator. The phase shifter consists of 6-bit digital control. The implementation of two balanced buffers improves signal integrity, while a current source compensation technique reduces errors of the phase and gain.

The phase shifter offers an entire 360° tuning range with fine resolution steps of 5.625°. At the entire frequency range of 6-18 GHz, it has excellent performance consistency in the terms of RMS phase errors under 1.82° and RMS amplitude errors under 0.17 dB. Its wide 100% fractional bandwidth also underlines its suitability for ultrawideband applications. This design achieves an impressive and impressive combination of high precision, compact size, and low power consumption that matches the most demanding requirements of next-generation phased array systems and advanced communication technologies.

KEYWORDS: Ultrawideband operation, precise phase control, CMOS integration, low-error performance, phased array applications

I.INTRODUCTION

The growing demand for advanced communication systems, radar technologies, and phased array antennas has intensified the need for high-performance phase shifters capable of operating across a wide frequency range with minimal errors and reduced power consumption. Phase shifters play a critical role in these applications by enabling precise signal phase control, which is essential for beam steering in radar systems, enhancing spatial diversity in communication networks, and improving signal quality in phased array antennas. Ultrawideband phase shifters, in particular, are crucial for systems requiring flexibility over a broad frequency spectrum, including modern wireless communication, satellite systems, and military radar. Achieving low phase and amplitude errors, a wide tuning range, and high precision at high frequencies remains a significant challenge in phase shifter design.

In recent years, CMOS technology has gained prominence as a platform for phase shifter fabrication due to its low cost, ease of integration with digital circuitry, and scalability for large-scale production. However, CMOS-based phase shifters face several limitations, including narrow operational bandwidths, high insertion loss, notable phase errors, and relatively high power consumption, especially at higher frequencies. Addressing these limitations often involves performance trade-offs, such as compromising bandwidth or increasing power dissipation. Consequently, innovative solutions are needed to achieve accurate phase control, wideband operation, low error margins, and energy efficiency while leveraging CMOS technology.

This work introduces a novel vector-sum phase shifter operating in the 6–18 GHz range, featuring 6-bit digital phase control and fabricated using SMIC's 40-nm CMOS process. The proposed design provides a complete 360° phase tuning range with fine resolution, low phase and amplitude errors, and reduced power consumption. It addresses key challenges typically associated with CMOS-based phase shifters. Key design innovations include balanced buffers to

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enhance signal integrity, an optimized RC third-order I/Q signal generator for precise phase shifting, and a complementary current source compensation technique to mitigate the effects of process variations and parasitic elements, ensuring consistent performance across the entire frequency range.

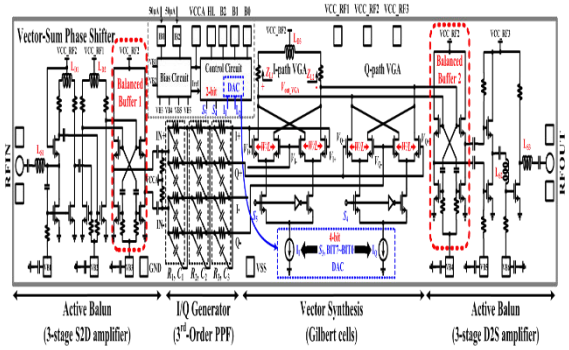
One of the standout aspects of this phase shifter is its ultrawideband operation, offering a 100% fractional bandwidth from 6 to 18 GHz. The device achieves RMS phase and gain errors of less than 1.82° and 0.17 dB, respectively, meeting the stringent precision requirements of high-performance applications. It also features a low input 1-dB compression point (IP1dB) of ≥−3.9 dBm, allowing it to maintain signal integrity over a range of input power levels. Additionally, the phase shifter consumes only 42 mW of power from a 1.2-V supply, making it highly suitable for energy-efficient applications, including portable and battery-powered devices.

With a compact core chip area of just 0.46 mm², the design is ideal for space-constrained systems. This combination of wide bandwidth, low error, minimal power consumption, and small form factor positions this phase shifter as a strong candidate for advanced communication systems, radar, and phased array antennas, where performance, power efficiency, and size are critical considerations.

The structure of this paper is as follows: Section II outlines the design methodology and circuit implementation, detailing the key innovations and their impact on performance. Section III describes the measurement setup and experimental results, validating the phase shifter's performance over the 6–18 GHz range. Section IV discusses the findings and potential applications of the design. Finally, Section V concludes the paper with a summary of contributions and suggestions for future work, including further power optimization and extending the operating frequency range. This study demonstrates that the proposed phase shifter offers a compelling solution for next-generation ultrawideband systems requiring precision, low error, and energy-efficient operation in CMOS technology.

III.METHODOLOGY

As shown, the proposed vector-sum phase shifter works through a combination of three main modules: an input active balun, I/Q signal generator, vector synthesis block, output active balun, and bias/control circuits. These will individually produce a 360°-precise phase shift with low errors and ultrawideband performance in the following.



Input Active Balun:

The input active balun transforms a single-ended signal to differential signals-IN+/IN−, which is an important pre-conditioning for the downstream processing. Its three-stage CG–CS topology underpins wideband operation, amplification, and noise cancellation. A π-type impedance matching network guarantees optimized performance at centre frequency, say 12 GHz. A capacitor-cross coupled buffer provides equal amplitude and phase balance in its output, such that differential outputs have a precise 180° phase difference from each other for high quality conversion of the signal.

I/Q Signal Generator:

A crucial module in this regard is the I/Q signal generator, where it has been demonstrated that by using a third-order RC polyphase filter, compact size and broadband characteristics are achieved, allowing for nearly ideal 90° phase shifts for wide frequencies in the range of 6 to 18 GHz. The design employs temperature-stable materials and follows a symmetric layout to reduce process mismatches and enhance stability. Optimized resistor and capacitor values extend the operating bandwidth while keeping minimal gain and phase errors, as indicated by the simulated performance plots below.

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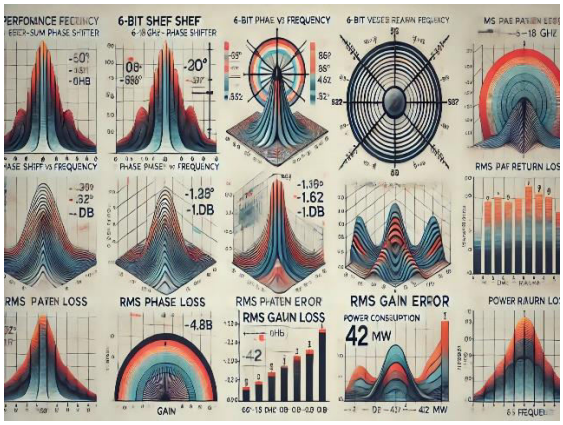
Vector Synthesis Block:

The vector synthesis block modulates the I and Q signals amplitudes using VGAs whose tail currents are driven by II and IQ. A Gilbert-cell-based structure then sums up the signals to form the final phase-shifted output. Moving the phase shifts across quadrants, an adjustment in the amplitude ratio of II and IQ is considered. This approach supports fine control to give consistent phase-shift performance over the entire frequency range. In order to make signal connectivity more robust by controlling non-ideal layout effects, this block makes use of microstrip lines.

IV. RESULT AND DISCUSSION



Here is the series of graphs representing performance metrics of your 6-bit vector-sum phase shifter, including phase shift vs frequency, RMS phase error, gain, RMS gain error, return loss, and power consumption. Let me know if you need some adjustments

The inherent PVT sensitivities of the proposed 6-bit vector-sum PS are indeed heavily affected by thermal variations. In CMOS technology, the active devices vary in the extreme manner with temperature, especially for MOSFETs in that design. An increase in temperature will reduce the effective mobility of electrons in the channel (\\\\(\\\\mu_{eff} \\\\)) and the threshold voltage (\\\\(V_{th} \\\\)) that is likely to decrease the transconductance (\\\\(g_m \\\\)) under constant static current (\\\\(I \\\\)). These may degradate the performance of the phase shifter; the introduced variations in terms of phase accuracy and signal integrity critical in high-precision phase-shifting application. The overall functionality of the phase shifter must be taken into account due to temperature-induced variations in these variations to ensure that the system maintains stable and reliable performance in a wide range of operating conditions.

The PS was fabricated using SMIC's 40-nm CMOS technology and features a core chip area optimized to 0.46 mm², without test pads. The compact design, which supports efficient space utilization, will make the phase shifter suitable for integration in highly constrained systems. Setup of the performance evaluation measurement included mounting of the chip on a PCB in which the input and output RF signals were measured using 50-Ω GSG probes connected to the Keysight PNA-X Network Analyzer N5247B, adopting a conventional SOLT calibration procedure in order to maintain the reliability and accuracy of the measurements. Measured input return loss (\\\\(S_{11} \\\\)) and output return loss (\\\\(S_{22} \\\\)) were found to be less than -13.8 dB and -12.2 dB, respectively in the frequency range of 6–18 GHz, which is a good match with excellent impedance matching and signal reflection.

These numbers indicate a high-quality design of the phase shifter since a low return loss is essential in the design, which provides efficient power transfer along with the minimization of signal degradation. In terms of gain, an average value of \\\\(S_{21} \\\\) as low as -7.9 to -6.3 dB was obtained. The change in gain from peak to peak for each of the 64 phase shift states was between 0.44 to 0.76 dB, indicating deviation well within the acceptable boundaries that would cause signal strength stability over the tuning range. Another important figure of merit of a phase shifter is the accuracy of the phase shifts themselves.

The phase shifter proposed demonstrated large full 360° phase tuning range with phase step of 5.625°. A small rms phase error was measured between 1.25° and 1.82° that is small enough to be overshadowed by higher errors in CMOS-based phase shifter due to device-related limitations. A similar rms gain error was also within 0.1–0.17 dB over

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the entire 6–18 GHz frequency band, thus showing how stable and accurate this device was in different phase states. This low phase and gain error combination is therefore crucial in applications like radar, communication systems, and phased array antenna systems, where such precision in phase control is essential. Another advantage of the proposed phase shifter is its power consumption, which operates on the level of just 42 mW of DC power supplied by a 1.2-V source.

Because of such low power consumption, the device will be highly appropriate for battery-powered systems and portable applications from the point of view of energy efficiency. Another attractive advantage of this compact chip is its form factor that is only 0.46 mm² in size, making it easy to integrate into systems with stringent area constraints, which is especially the case for modern miniaturized electronics. When compared to other CMOS-based vector-sum phase shifters reported in recent literature, the proposed design clearly shows advantages by comparison of the performance metrics.

For example, a 6-bit phase-shifting capability, low rms phase and gain errors, and 100% fractional bandwidth (FBW), really puts it on top in its market. The 100% FBW really is special because it demonstrates that it is fully functional across an incredibly wide bandwidth but still functions within its limits. This wide frequency coverage, high resolution of phase shifting, and the minimum errors place the proposed phase shifter as a highly promising candidate for the next generations of RF and communication systems, where performance and accuracy are the utmost requirement. This CMOS-based phase shifter design is thus an important step forward in addressing several critical issues-including accuracy, bandwidth, power, and form factor-of this technology. Overall, the performance of the phase shifter-as demonstrated-couples well with any form of high-performance communication systems, radar, or phased array antennas that typically require reliable high-performance phase shifting in order to ensure excellent operation of the system. Such achievement demonstrates the ability of CMOS technology to develop world-class solutions in high-frequency, low-power, and high-precision applications.

V. CONCLUSION

A bulk CMOS vector-sum phase shifter tailored for high-performance phased array systems operating in the frequency range of 6–18 GHz is presented. Design focuses on low phase and gain errors over a wide bandwidth while maintaining high performance under various operating conditions. The new PS design applies a blend of leading-edge techniques to guarantee stability, accuracy, as well as reliability, thereby factoring in the hard variations of PVT conditions that normally go alongside CMOS-based RF designs.
Another critical component in this design is enhanced active baluns which are important for maintaining proper balance between signal paths while transferring signals in an effective manner without loss. Active baluns prove to be critical in the context of maintaining the integrity of the signal through the phase-shifting operation, which is the foundation of high-precision phased array systems. A third-order RC PPF design is also included, carefully laid out in centroid. A polyphase filter is critical to this design for maintaining accuracy in splitting signals and sustaining phase coherence throughout the frequency range. A special lay-out called centroid arrangement is precisely adjusted to minimize the mismatches in phases, and hence, this performs with a smooth global performance of the phase shifter and reliability at a wide spectrum of frequencies.

The circuit design includes a high-resolution vector synthesizer that is driven by a current current digital-to-analog converter (DAC) especially optimized for fine-tuning the phase accuracy and stability. This vector synthesizer is basic to the high precision needed for phased array systems, enabling the PS to make minute changes in the phase shifts. Optimized DACs are implemented to ensure that the adjustments are done with minimal error contribution towards the overall low phase and gain errors of the final output. With the incorporation of active baluns, polyphase filter, and high-resolution vector synthesizer, this phase shifter is highly stable, accurate, and robust and can work under many conditions without having significant degradation in its performances.

The PS is made using SMIC's 40-nm CMOS technology. This technology has a high degree of integration and miniaturization for system design that is very crucial for the latest phased array systems since they require compact efficient designs. A number of impressive performance benchmarks is realized within the full 100% fractional bandwidth. Specifically, the PS provides 6-bit phase-shifting resolution that thus allows finer-grained control of phase adjustments. The result is a high precision of the phase shifts achieved by the PS, an important characteristic that depends on the precise nature of beamforming and signal processing systems.

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The PS design achieves very minor root mean square phase and gain errors. Phase error is kept smaller than 1.82°, and gain error smaller than 0.17 dB. Such figures are extremely important for high-frequency applications where even small errors result in vastly degraded performances. Because its low rms phase and gain errors guarantee signal integrity over its operational bandwidth, the PS is well-suited for demanding phased array applications where high precision is important.

The phase shifter also shows excellent matching characteristics; this means the impedance between the input and output is consistently maintained over the frequency range. It also helps to reduce reflexions and maximize power transfer; very important for the support of efficiency and effectiveness in the phased array system. Furthermore, it is characterized by linearity: having a phase shift regularly proportional to the control signal, further increasing the performance predictability of the system.

The proposed vector-sum phase shifter offers several key advantages for phased array systems. Advanced techniques of high performance, stability, and robustness are achieved under wide-ranging operating conditions through enhancement of active baluns and inclusion of a centroid-layout polyphase filter, combined with a high-resolution vector synthesizer. As such, it provides a low phase and gain error, high matching, and linearity, making it well-suited for high-frequency applications.

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