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Designing of BCH Decoder Using Novel Folding Technique

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ABSTRACT: Till date, various techniques have been employed to enhance the quality of data transmission in optical network. Among those approaches, Forward error correction (FEC), or commonly called error correction coding (ECC), is viewed as the most cost-effective solution, and has been widely adopted in many industrial optical transmission systems. Many specific FEC codes, including Reed-Solomon (RS), BCH, and LDPC codes, are proposed in different industrial standards for error correction in physical layer. Present VLSI has demand to improve the performance of the digital circuits. We have target to enhance the performance of Bose-Choudhuri-Honquenghem (BCH) decoder. So existed BCH decoder has been implemented using Galois Field (GF) conventional multiplier in processing element which is having much critical path delay and area. The proposed technique is reduced those parameters with the help of folding processing element (with novel folding technique) is placed instead of processing element. Here GF multiplier generates output is represented in Key Equation Solving (KES) method. The design is implemented using XILINX 14.7 ISE software with ARTIX-7 FPGA.

KEYWORDS: Forward Error Correction (FEC), Bose-Choudhuri-Honquenghem (BCH) Decoder, Galois Field (GF), Key Equation Solver (KES)

I. INTRODUCTION

Generally, in high-speed optical communication, the increase on data rate usually comes with the increase on signal bandwidth and sampling rate. In this case, due to the sensitiveness of optical and electronic devices, the additive transmission noise will inevitably increase as well. Therefore, how to increase the throughput of optical network without loss of robustness is an essential task when designing modern high-speed optical network.

The digital data bandwidth used in communication or audio-video systems is rapidly increasing [12]. The advantage of digital signals over analog signals is that they aremore reliable in a noisy environment, since for each symbol the detector in a digital system only needs to detect either a ’1’ or a ’0’ [2].If the data are carried over a noisy environment and the strength of the noise is enough to change value of the original data symbols, then the detector might make an erroneous decision. However, if the data is *coded*, by adding appropriate check (redundant) symbols to the data symbols, the receiver (including detector and decoder) can detect, and possibly correct certain errors, making the signal reception more reliable. Adding redundant check symbols to data symbols is called *errorcontrolcoding* [2]. It is often referred to as a FEC technique, which is widely used in digital and real-time communication systems. FEC implies that the error-correcting code is applied to the data prior to transmission, and bit errors occurring during transmission are corrected at the receiving end of the system. One of the disadvantages however is that if the number of bit errors is higher than the error-correcting capability of the FEC decoder, then the uncorrected bit errors will remain in the decoded data [2].Based on the error-correcting capability.To decode BCH codes a BCH decoder is needed, see Fig 2.3. Input to the BCH decoder is the message received from the channel, *r(x)*.

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First step in the decoding process is the computation of the syndromes. Syndromes serve only as error indicators, i.e., they will notify us of error occurrence but not of position of the error(s).
To be able to correct the erroneous bits, we need to know the position of those. By utilising the computed syndrome, an error-location polynomial, *_(x)*, can be calculated using the Berlekamp Massey algorithm (BMA) [3]. Error positions are roots of the error-location polynomial and are found with Chien search, see Sec. 2.2.3.3. Output of the Chien search is an error position vector *e(x)*,that indicates position(s) of erroneous bit(s) with a one [3, 1].Since its discovery, Bose-Chaudhuri-Hocquenghem
(BCH) codes are widely used in numerous communication and storage systems, such as second generation Digital Video Broadcasting (DVB-S2), optical fiber communication systems, NAND flash memory controllers and so on.Compared to Reed-Solomon (RS) codes, BCH codes achieve additional coding gain of around 0.6dB [1] with similar code rate. In addition, characteristics of the binary codes can help to reduce the hardware complexity [2].
This work provides the high speed and low area BCH decoder design resulting from the efficient KES module.
From the following graph, how much of leakage power increasing when technology becomes scale down [2]. Mobile-multimedia applications have two operation modes, active mode and standby mode. For example, mobile have low activity factor where their idle time is larger than active time. In ideal time, these devices effected by the leakage power loss which reduces the battery service time, to address different leakage power optimization techniques have been developed.

II. MODIFIED DESIGN ARCHITECTURE

For the practical long BCH decoder, the SC and CS still dominate the processing cycles even if they are massively parallelized [11]. Hence, the area-efficient folding scheme is
normally applied to the KES stage while maintaining the throughput [1]. In the previous *t*-folded SiBM structure in *t* processing elements (PEs) are shared by expanding the processing cycles from *t* to t^2. Through this brief, we call this PE-level folding as global folding since it keeps the original PE structure. Note that the global folding factor, which is denoted as *fG*, can be increased up to 2*t* [6]. Although global folding may relax the complexity in effect, it still suffers from the long critical path caused by the conventional multiplier, limiting the clock frequency.
Existed GF multiplier whose inputs are two arbitrary *m*-bit GF elements in polynomial forms, i.e., $a(z) = a0 + a1z + \cdots + am-1zm-1$ and $b(z) = b0 + b1z + \cdots + bm-1zm-1$, where *m* stands for the field dimension. Similarly, the output of the multiplier is represented as $c(z) = c0 + c1z + \cdots + cm-1zm-1$. The primitive polynomial is denoted as $p(z) = p0 + p1z + \cdots + pmzm$. Note that $p0 = pm = 1$ by definition [3]. Every full adder and half adder blocks in GF multipliers are represented with type-0 and type-1 cells. Cells in figure 2 reduce the critical path delay in in existed GF multiplier. Delay of the cell1 is represented as *T*AND + *T*XOR and cell2 represented as *T*AND+ *T*XOR + *T*XOR. KES based GF multiplier in figure 3 is placed in processing element (figure4).

Two multipliers and one adder and one MUX units are observed in the processing element (figure 4). Two multipliers are placed with GF multipliers. Multiplied outputs are added then output is taken as deltai represented in the figure. One of the inputs is selected by using MUX at tetai+1. This PE block is placed in the SiBM architecture in figure1. SiBM is used to decode the error data.

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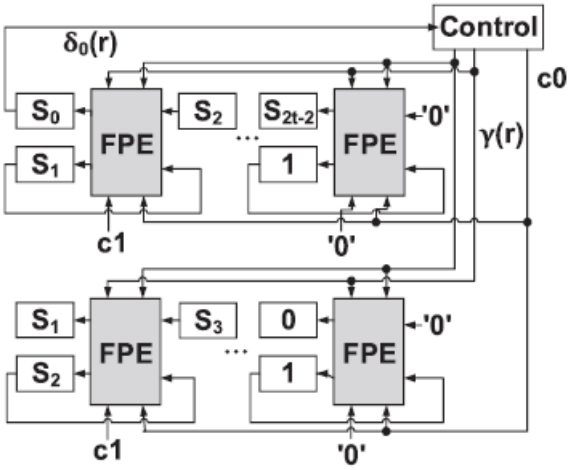

Fig 1.SiBM architecture

In the same SiBM architecture existed GF multiplier is replaced with the proposed 4-fold GF multiplier is shown in figure 5. Proposed multiplier 4 cells and one MUX but in existed multiplier have total eight type0 cells and 8 type1 cells. Area is increased in the existed design than proposed design multiplier. Critical path of the proposed design reduced than existed multiplier.

Similarly proposed PE block also gets same advantage than existed PE block. PE and Multiplier waveforms are represented in figures 6 and 7.

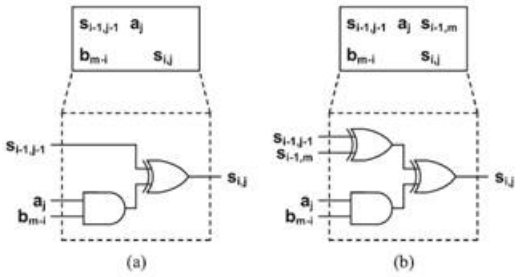

Fig2.(a) type0 cell (b) tpe1 cell

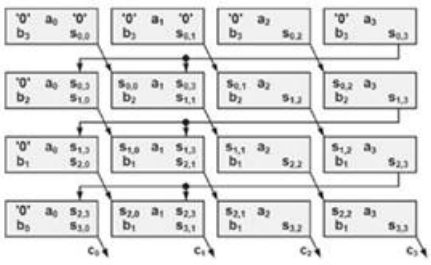

Fig3.Existed GF multiplier

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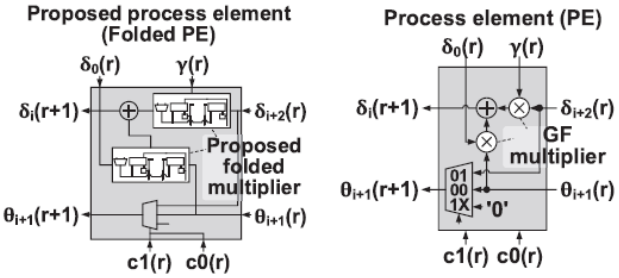

Fig 4.(a) Proposed PE (b) Existed PE

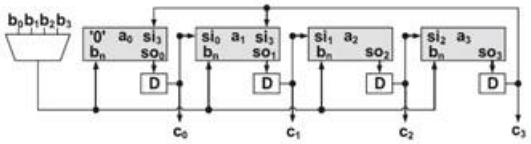

Fig5. Proposed GF multiplier

III.RESULTS AND CONCLUSION

Fig 6.Output Waveform of existed GF multiplier

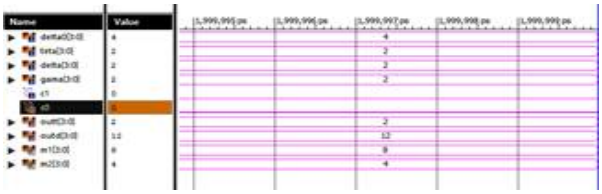

Fig 7.Output Waveform of proposed GF multiplier

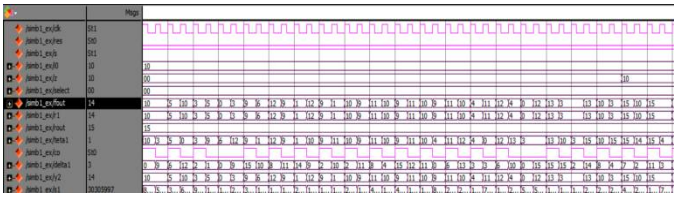

Fig 8.Output Waveform of proposed BCH decoder

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Table 1: Existed Vs Proposed Multipliers Analysis

	LUT	IOB	Delay
Existed Multiplier	8	12	6.801nS
Proposed Multiplier	5	16	1.473nS

Table 2: Existed Vs Proposed Processing Elements Analysis

	LUT	IOB	Delay
Existed PE	32	26	7.960Ns
Proposed PE	16	30	1.507Ns

Proposed design is implemented using Xilinx 14.7 with SPARTAN6 FPGA. Output of processing element and multiplier is shown in above figures 6 and 7. Proposed and existed designs area and power analysis is compared in the above table. Proposed design gets better results due to that we proposed area efficient and high speed designs for BCH decoder.

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