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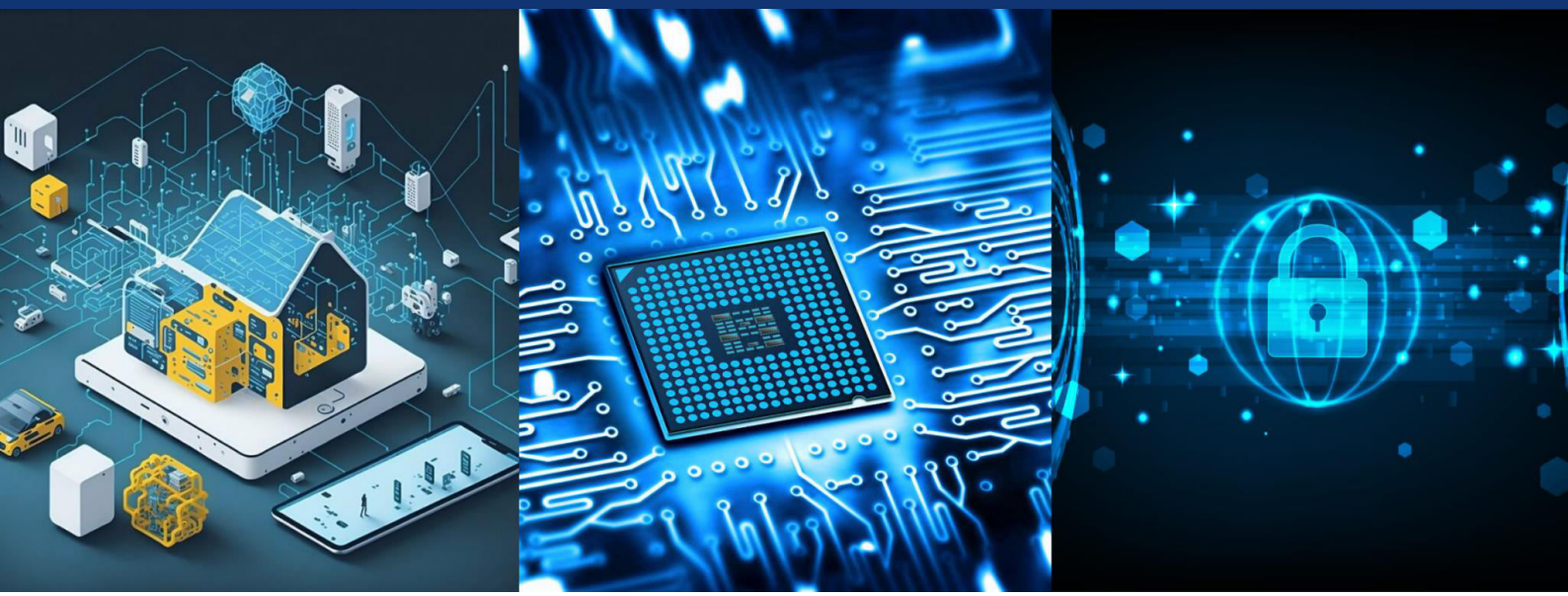

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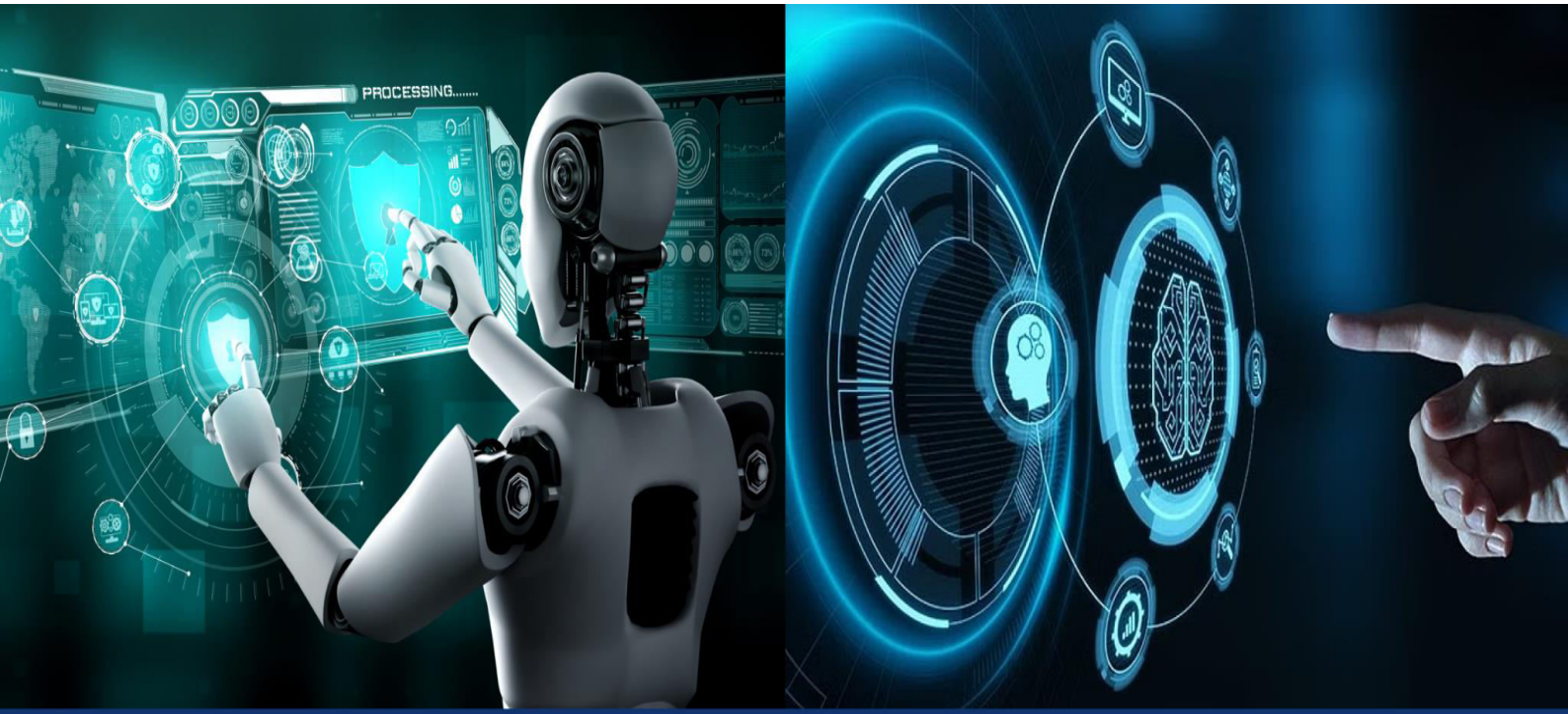

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A 32-Bit Ripple-Ling Hybrid Carry Adder

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ABSTRACT: this project we were effectively managing the carry generation and propagation paths of the hybrid adder achieves improved speed and efficiency while maintaining a achievable circuit complexity. Simulation results demonstrate that the 32-bit Ripple-Ling Hybrid Carry Adder performs like a conventional RCAs in terms of both propagation delay and power consumption, making it a practicable option for high-speed arithmetic operations in modern computing systems. Further research in this project optimizes the hybrid adder's parameters reduce in number of ripple-carry stages which further reduce in delay, area, and power.

KEYWORDS: Adder, ripple carry, Ling carry, low power, low cost

I.INTRODUCTION

As device sizes continue to shrink to the Nano meter scale, the use of low power techniques has become more important than ever for the design of any complex VLSI chip like microprocessors and DSPs, which encompass various complex arithmetic operations such as subtraction, multiplication, division, and addition. They are typically implemented using one or multiple addition operations. Therefore, adders are the most used arithmetic units in complex VLSI chips Adders often reside on the critical path of digital circuits, directly affecting the overall speed of the system. Hence, optimizing the area, power consumption, and operation speed of adders is crucial for enhancing the performance of the entire system So far, significant research efforts have been devoted to shortening the critical path in multi-bit addition, which mainly focus on the optimization of sub-units in 1-bit full adder and the whole carry structure. In terms of customizing sub-units in 1-bit full adder Naseri and Timarchi use XOR/XNOR gates based on transmission gate (TG) to realize six new hybrid 1 bit full-adder circuits. This design performs well when implementing 2- to 4-bit adders. However, the TG structure is unsuitable for cascading adders with a bit width exceeding 16, due to the substantial increase in delay.

II. EXISTING METHOD

The Ling adder proposed in as depicted in Fig 1 consists of a 32-bit adder divided into four summing blocks. Each summing block is further divided into multiple summing groups. Specifically, Bit 8:0, Bit 17:9, and Bit 26:18 all have three summing groups, while Bit 31:27 are divided into a 3-bit summing group (Bit 29:27) and a 2-bit summing group (Bit 31:30). The carry signals, H_2, H_8, H_{17}, and H_{26}, between the blocks are generated by a global look- ahead carry block. Fig 2.1 illustrates the structure of the Global Look-Ahead Carry module in Fig 1.1 To generate the block carry signals, H_2, H_8, H_{17}, and H_{26}, the group carry generation signals G_i^* and propagation signals P_i^* are first generated. Then, H_8, Gb_i^* and Pb_i^* are generated based on P_i^* and G_i^*. Finally, the carry signals H_{17} and H_{26} are generated based on $Pb_i^*$and Gb_i^*.Let $A_{31\sim0}$ and $B_{31\sim0}$ represent the two 32-bit input binary numbers, and $S_{31\sim0}$ represent their output sums.

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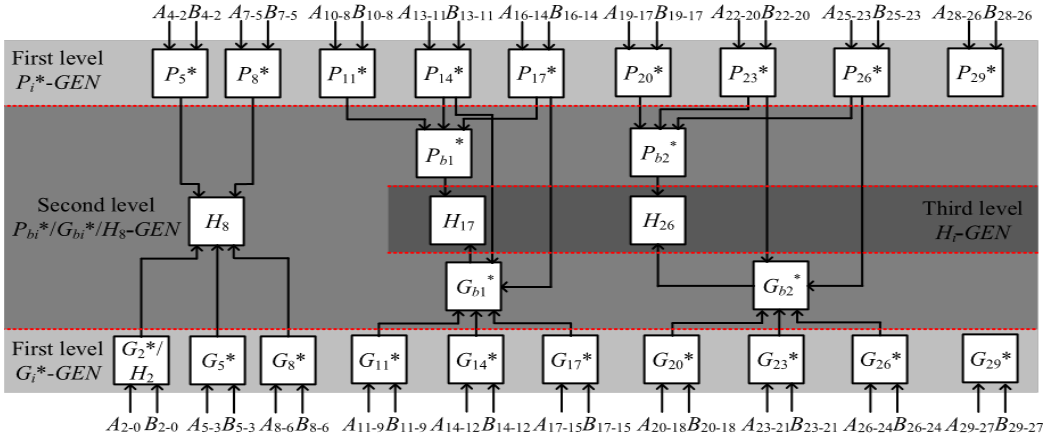

Fig 1 The carry tree for ling adder

III.PROPOSED METHOD

The circuit will be optimized in the following two aspects. First, custom designed compound logic gates, such as NAND, NOR, and XOR-mixed gates, as well as the custom designed $A_i B_i + X(A_i \oplus B_i)$ operator, are used to achieve area optimization while ensuring fast computation. Next, in order to reduce the delay of output sum with long paths, such as S_{26}, we optimize the Shannon expansion variables to align the delays of control and input signals for the final MUX, further reducing overall latency.

(a) **XOR-NAND-NOR Mixed Logic Gate**

Firstly, we propose a compact circuit that simultaneously realizes XOR, NAND, and NOR operations. The XOR logic is the most commonly used arithmetic unit in addition logic.

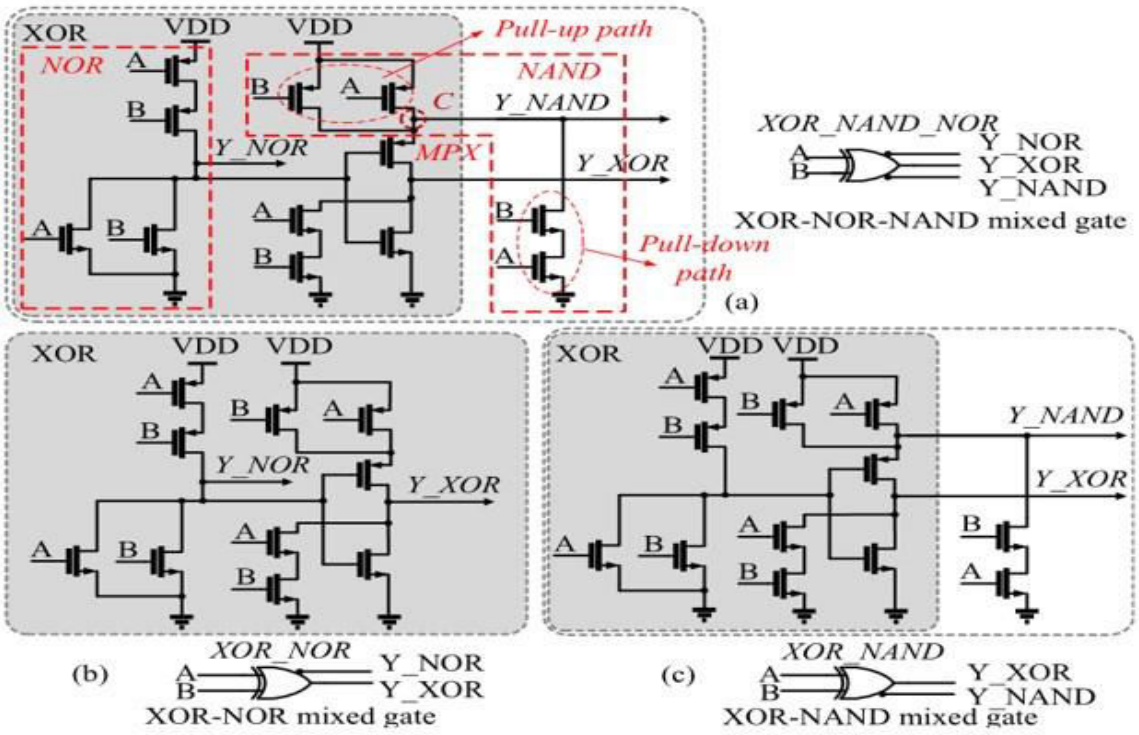

Fig 2 (a) XOR-NAND-NOR (b)XOR-NOR(c)XOR-NAND mixed gates

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(b)**C_i – GEN**

As the output carry C_i using the ripple structure is commonly expressed as $A_i B_i + C_{i-1} (A_i \oplus B_i)$. If standard logic gates are used to generate this signal, as shown in Fig 3 it would require two AND gates, one OR gate, one XOR gate, and three inverters.

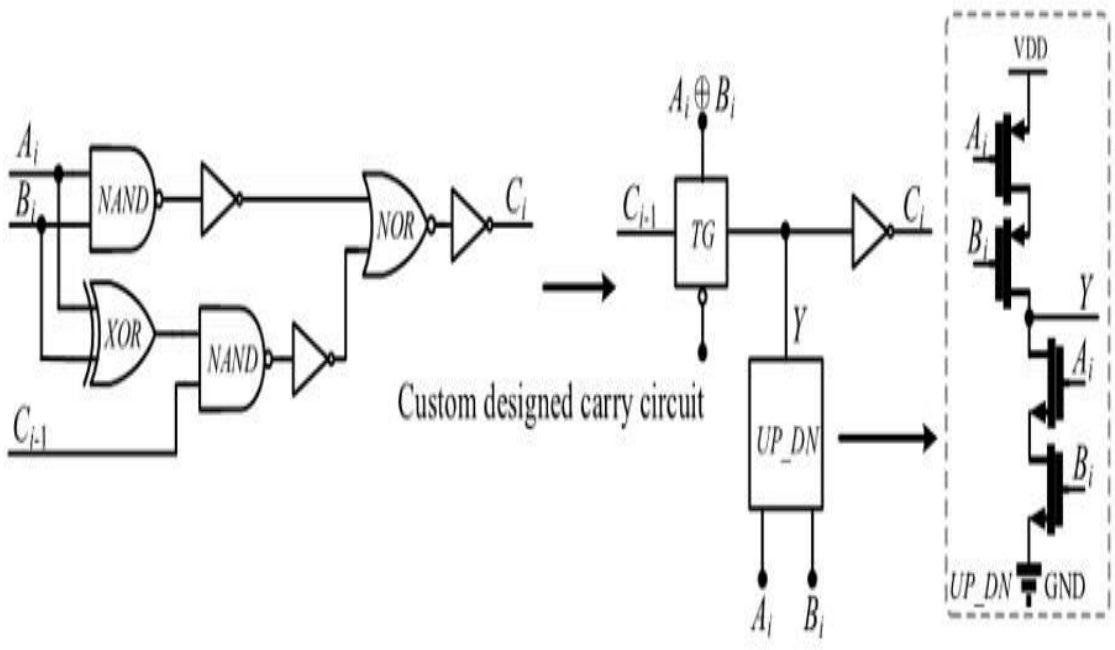

Fig 3 Custom design to realize *Ci-GEN*.

(c) **Optimization of Shannon Expansion**

As discussed in Section the conventional method that treats the block carry signal H_{17} as a variable for Shannon expansion cannot realize delay balance for the realization of S_{26}, and we can appropriately increase the delay of the control signal and decrease that of the input signal for the output MUX.

(d) **Output Sum Generation Circuit for Each Bit**

Next, we will generate the output sum for each bit using the optimization methods mentioned above. For the output sum generation circuit of Bit 2, according to Fig 2.2 the local bit sum s_2 needs to be XORed with the carry signal C_1 to obtain the output sum S_2. To further simplify the circuit, as shown in Fig 4.4 we use the MUX composed of two TGs to implement the final XOR logic, in which s_2 acts as input signal and $C_1$is the control signal. An inverter is added to the output of MUX to obtain the final S_2 and ensure its output driving capability

IV.SOFTWARE REQURIMENTS

Software requriments : Xilian vivado

VLSI Design flow

The VLSI design cycle starts with a formal specification of a VLSI chip, follows a series of steps, and eventually produces a packaged chip

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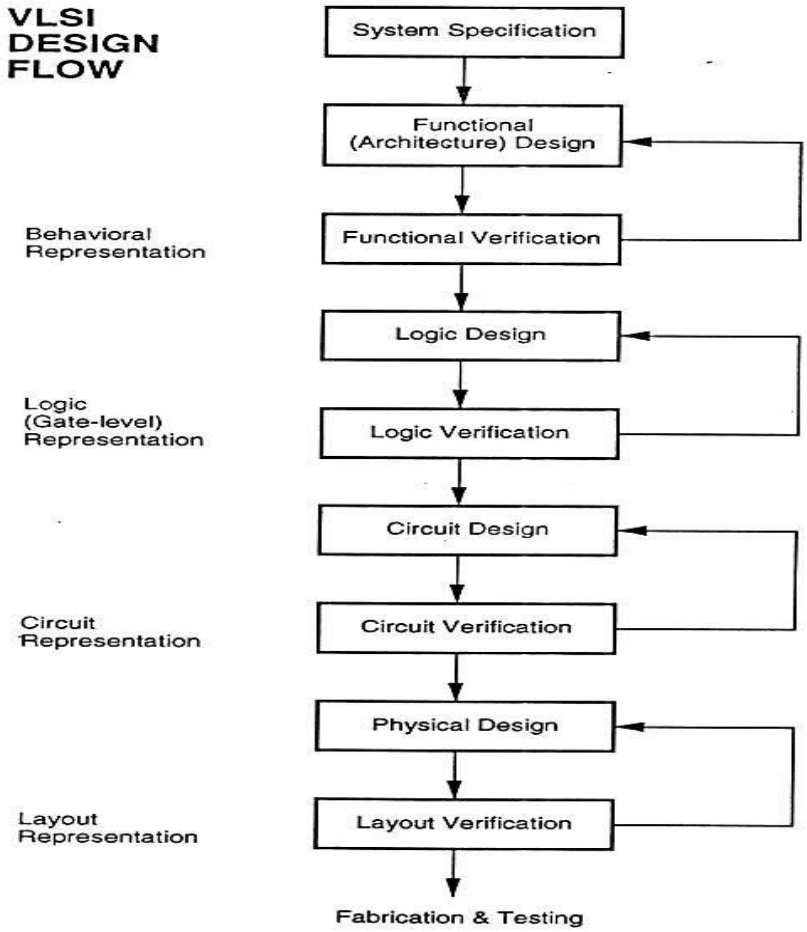

Electronic Design Automation (EDA) software

EDA software is used to automate the design and simulation of electronic circuits. It allows engineers to create and test different designs virtually, without the need for physical prototypes.

Layout editors

Layout editors are used to design the physical layout of the circuit, including the placement of individual components and the routing of wires and connections.

Verification tools

Verification tools are used to ensure that a VLSI design meets all of the necessary specifications and requirements.

Fabrication tools

Fabrication tools are used to create the physical version of the VLSI design, including the mask layout and the photomask used in the manufacturing process.

V.APPLICATIONS

1. Digital signal processing
2. Microprocessor design
3. FPGA and ASIC Design
4. Arithmetic Logic Units
5. Image Processing
6. Graphics Processing Units

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VI.RESULTS

The ripple and ling carry adder are performed area and delay and power using ling method. the 32-bit ripple-ling hybrid carry adder serves as an effective and efficient component in digital arithmetic, contributing to quicker computation times and better performance in integrated circuits, thereby fulfilling the increasing demands for speed and efficiency in contemporary electronic design

COMPARISION BETWEEN EXISTING AND PROPOSED METHOD

PARAMETERS	EXISTING ADDER	PROPOSED ADDER
Area	No of transistors=3188[11]	88LUT
Power consumption	31.327 W [11]	22.4 W
Delay	49.95 ns [11]	29.2 ns

VII. CONCLUSION

The 32-bit ripple-ling hybrid carry adder demonstrates a balanced approach to arithmetic operations in digital circuits by effectively merging the principles of ripple carry addition and carry lookahead techniques. This architecture leverages the simplicity and low gate count of ripple carry adders while enhancing performance through the implementation of a carry lookahead mechanism, significantly reducing the carry propagation delay. The hybrid design results in improved speed compared to traditional ripple carry adders, particularly for larger bit-width operands, making it suitable for high performance computing applications where fast addition is critical. Additionally, this adder can be optimized for Delay,area and power consumption.

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