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Power Efficient Sense Amplifier Using CMOS 130nm Technology

V.Bhandhavi[1], S.Sridhar[2], M.Ramya[3], G.Mounika[4], T.Poojitha[5], R.Mahesh Reddy[6]

B.Tech, Dept. of E.C.E, D.M.S.S.V.H College of Engineering, Machilipatnam, India[13456]

Assistant Professor, Dept. of E.C.E, D.M.S.S.V.H College of Engineering, Machilipatnam, India[2]

ABSTRACT: In modern computer memory, a sense amplifier is one of the elements which make up the circuitry on a semiconductor memory chip (integrated circuit); the term itself dates back to the era of magnetic core memory. In this paper we have designed Faster & Power Efficient Sense Amplifier for CMOS SRAM using VLSI Technology. Schematic of the sense amplifier design is implemented using mentor graphics 130nm (PYXIS GDK) technology and layout also done for the proposed design. Our focus will be to reduce the transistor count, to improve the power consumption, power dissipation and also to improve the response time of sense amplifier

KEYWORDS: Integrated circuit, Sense amplifier

I. INTRODUCTION

Semiconductor memories are usually considered as the most vital components of digital logic system design for computers, microcontrollers, DSPs and other microprocessor based applications. In recent years there has been an increased tendency to embed the memory (RAM and ROM) in the logic circuit, to achieve higher levels of integration and speed. **As** a result, the performance of the memory array and the limitations of the memory periphery circuitry (decoders, charge pumps, level shifters, sense amplifiers) can seriously affect the overall system performance in terms of power dissipation and speed. One of the most critical circuits in the periphery of a memory is the sense amplifier **(SA).** A sense amplifier is part of the read circuitry that is used when data is read from the memory; its role is to sense the low power signals from a bit line that represents a data bit (1 or 0) stored in a memory cell, and amplify the small voltage swing to recognizable logic levels so the data can be interpreted properly by logic outside the memory.

Sense amplifiers are strongly related to the access time of memory, as they are used to retrieve the stored memory data by amplifying small signal variations in the bit-lines. Designing fast, low-power and robust sense amplifier circuits is a challenge, especially in the area of submicron CMOS technologies, because in modern memory designs bit-lines tend to exhibit significant capacitance. **As** a result they severely limit the sensing speed by introducing extra signal delays. Furthermore, the small signal voltage gain provided by submicron transistors decreases as the channel length becomes smaller, owing to channel length modulation. A comparison of different current mode sense amplifiers using 0.25 pm CMOS technology is presented in [6]. While significant variation challenges exist for technologies past 32nm, numerous solutions are being explored to drive Moore's Law forward.

Process variation is not an insurmountable barrier to Moore's law, but is simply another challenge to be overcome. Scaling improvement is described in [2]. In paper [5] describes about comparative results between current mode and voltage mode sense amplifiers. Present results [6] on how the two sense amplifier behave for the two design topology for low power (LP) process technology optimized for mobile low leakage application and the second one is high performance High Performance (HP) applications. Detailed Spice simulation with statistical models and Monte Carlo simulations is utilized to compare the two designs for active power, leakage power, speed, and area. Our study shows that VLSA performs better than CLSA - being 67% faster, 35% smaller area, and similar active power for the LP. The VLSA also performed better than the CLSA is the HP technology as well. Modified design enhances the sense

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amplifier design which gets better results. We refer the traditional sense amplifier and measure the analysis of same design and modified design. Modified design gets improve area and power than traditional sense amplifier.

II. PROPOSED DESIGN ARCHITECTURE

The sense amplifier used to read data from the cell. As soon as the SE signal goes HIGH, the sense amplifier senses the appropriate difference between the BIT and ~BIT voltages and produces an output voltage. The access time of the memory, which is defined as the time between the initiation of the read operation and the output, mainly dependent on the performance of the sense amplifier? So the design of the sense amplifier is the main criteria for the design of memories [6]. When SE is high (in figure 1), output of the sense amplifier is equal to bit. Here inputs of the sense amplifier are Sense Enable (SE), BIT, BIT BAR. For example SE=1, BIT=1 and BIT BAR=O then output=1. In voltage sense amplifier total transistor count is 7.The amplifier is composed of a differential pair (Transistors M1 and M2) with an active current mirror load(M3 and M4) and a biasing source(M5)

In figure 1 SE (y) = 1 and BL (x) = 1, BLB (xb) = 0, transistor M7 and M4 are ON and also M6 is OFF. Due to these inputs, path is established between ground (0) to inputs of the transistors M1 and M2 through M7 and M4. Here both the transistors M1 and M2 are ON then Vdd is passed to the output [z] through the transistor M2.output of the modified design is 1 which is equal to both the inputs SE (y) and x and output bar (zbar) is equal to input bar (xb). In case of both the inputs (SE and x) are equal to zero then we get output as zero and output bar as one. Our design is senses the input data when sense enable is high which is also called as read the data from cell. Now enhance the performance of the design in terms of power dissipation, power consumption and also transistor count.

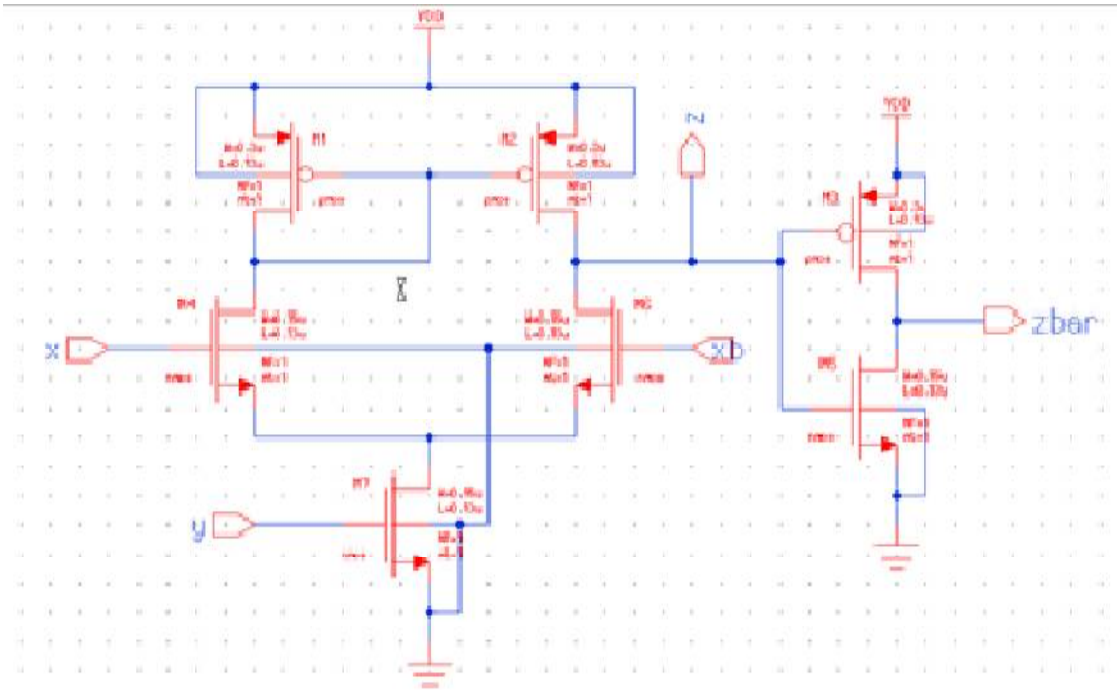

Figure 1: Voltage Sense Amplifier

Fig2 represents the output waveforms of the voltage sense amplifier where wave forms are formed by mainly 3 steps bases on the x manager tool ,in this tool mainly waves are observed after the completion of those steps are 1)schematic

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designing 2)Test bench(symbol generation),3)Analysis.Finally on analysis we will get the required output wave forms which are shown below

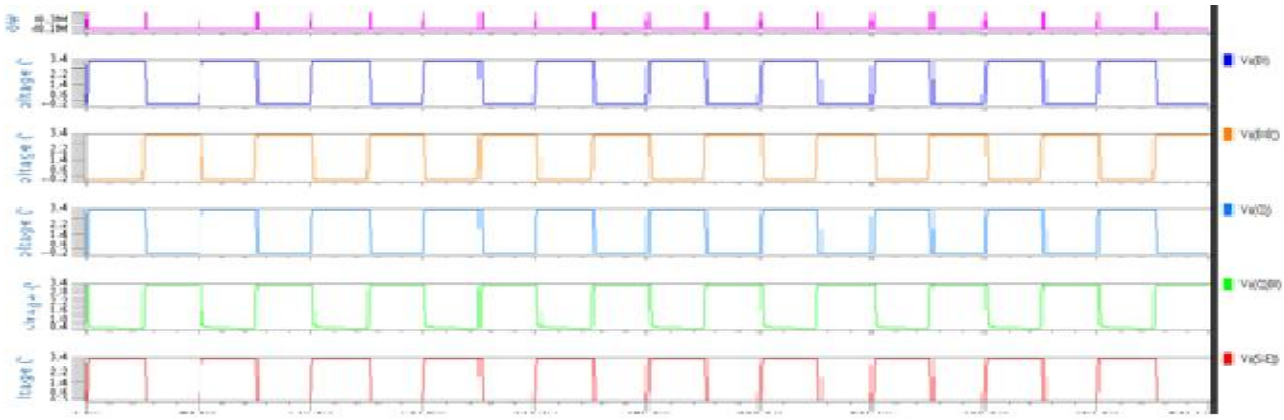

Figure 2: Waveform of Voltage Sense Amplifier output

III. EXISTING SYSTEM

Modified sense amplifier and existed sense amplifier outputs are observed in figures 3 and 4. Physical design and verification (Design
Rule Check), schematic versus layout and parasitic extractions of those amplifiers is done by using calibre tool in the PYXIS environment.
Power consumption of modified design is reduces up to 98.84% than existed sense amplifier design. And also third one is bar graph in figure 6 which represents transistor count between same designs. Transistor count is directly proportional to area so area of the voltage sense amplifier is less than the traditional sense amplifier.

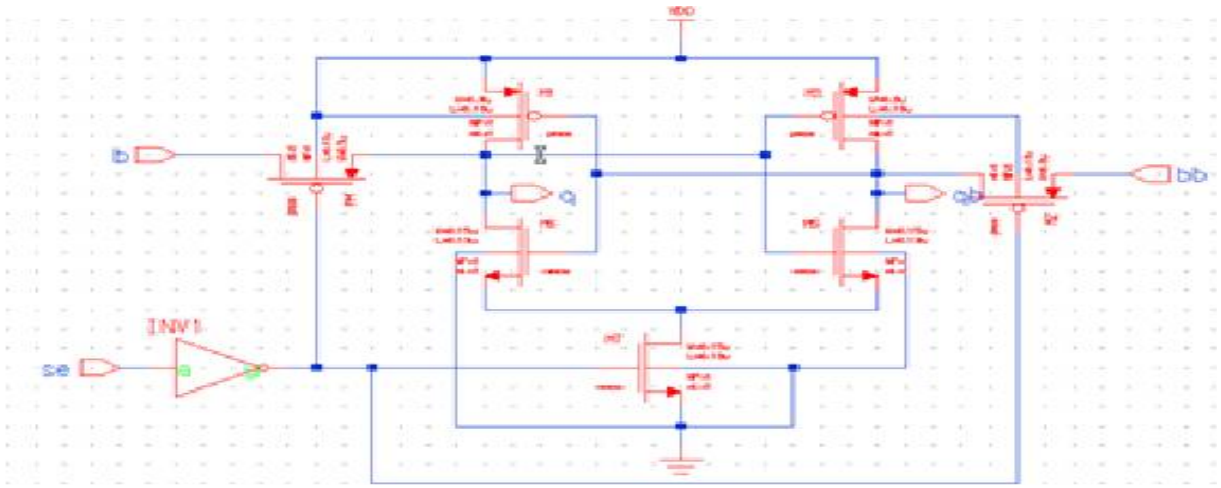

Fig3. **Traditional Sense Amplifier**

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Output waveforms of the traditional amplifier is shown in following figure4.

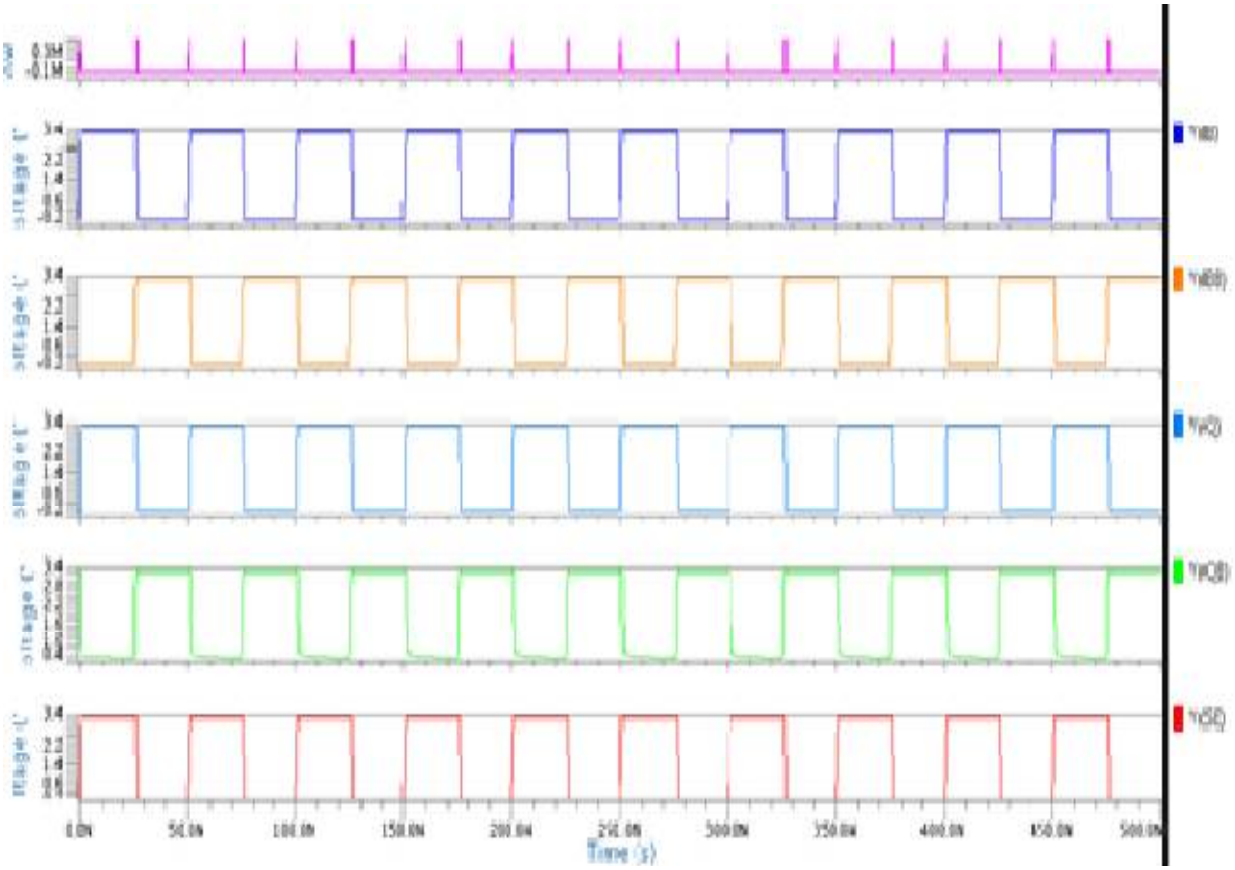

Figure 4: Waveform of Traditional Sense Amplifier output

IV. METHODOLOGY

Sense amplifier designs are implemented using Mentor Graphics 130nm technology. Comparison results are represented with pie and bar graphs. First bar graph in figure 4 represents power dissipation between existed and modified designs, modified design reduces the power dissipation 98.85% than existed design at supply voltage=2.2v.
Figure 4: Power Dissipation comparison between Voltage and Traditional Sense Amplifier
Second bar graph in figure5 represents the power consumption at vgs=2.2v and vdd=2.2v between same two designs. Power consumption of modified design is reduces up to 98.84% than existed sense amplifier design.

RESULT-(1)
On drawing pie chart of the power consumption between the voltage mode sense amplifier and traditional mode sense amplifier is shown in the figure

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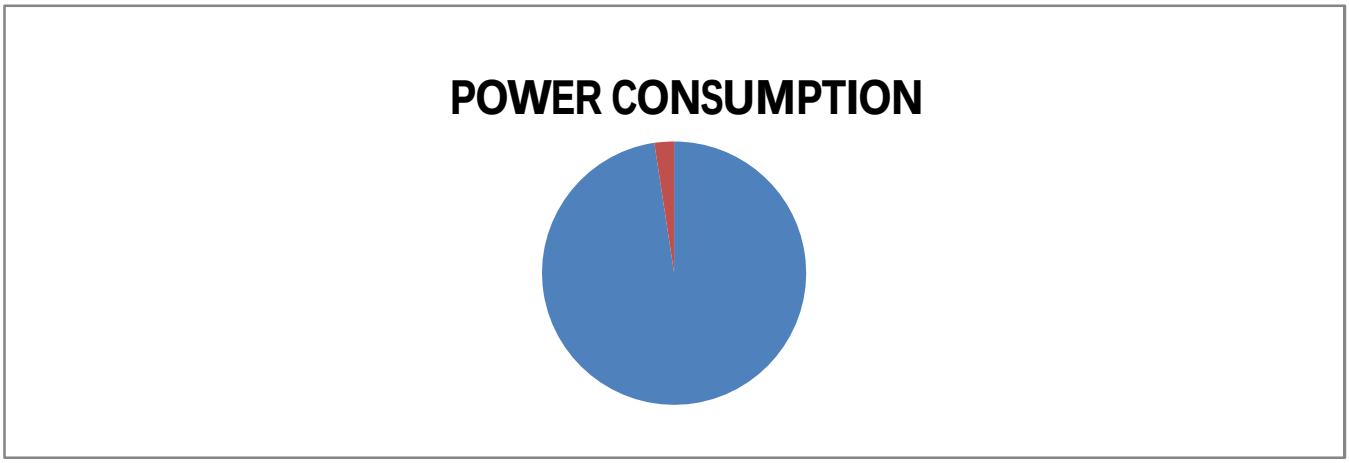

Fig5. Power Consumption comparison between Voltage and Traditional Sense Amplifier

RESULT-(2)
On drawing the power dissipation comparison the between voltage mode sense amplifier and traditional mode sense amplifier is shown in the figure6

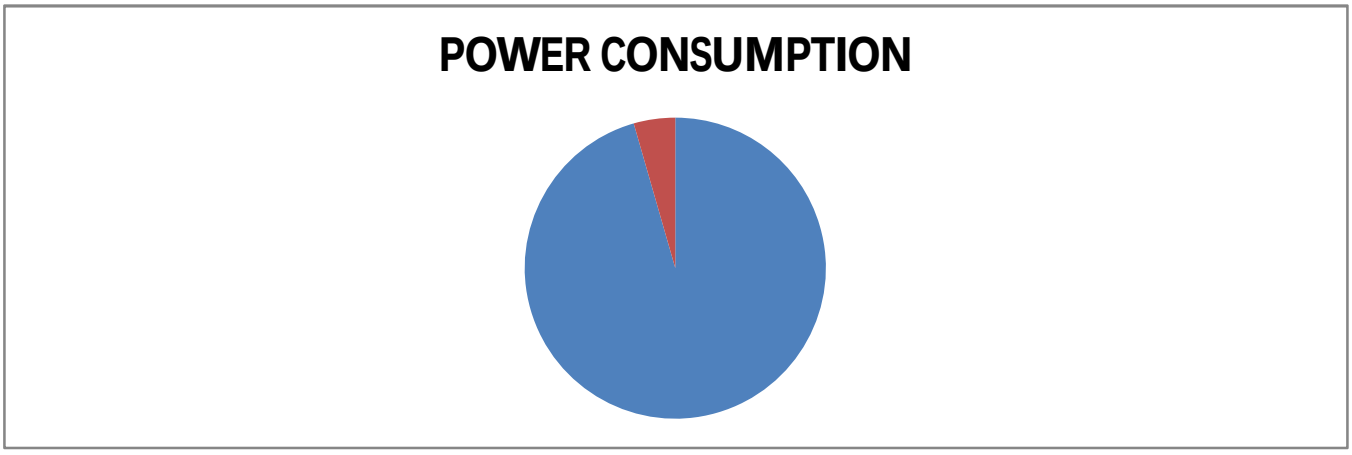

Fig6. Power Dissipation comparison between Voltage and Traditional Sense Amplifier

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figure 7 which represents transistor count between same designs. Transistor count is directly proportional to area so area of the voltage sense amplifier is less than the traditional sense amplifier.
Finally voltage sense amplifier or modified design improve the performance results than existed design.

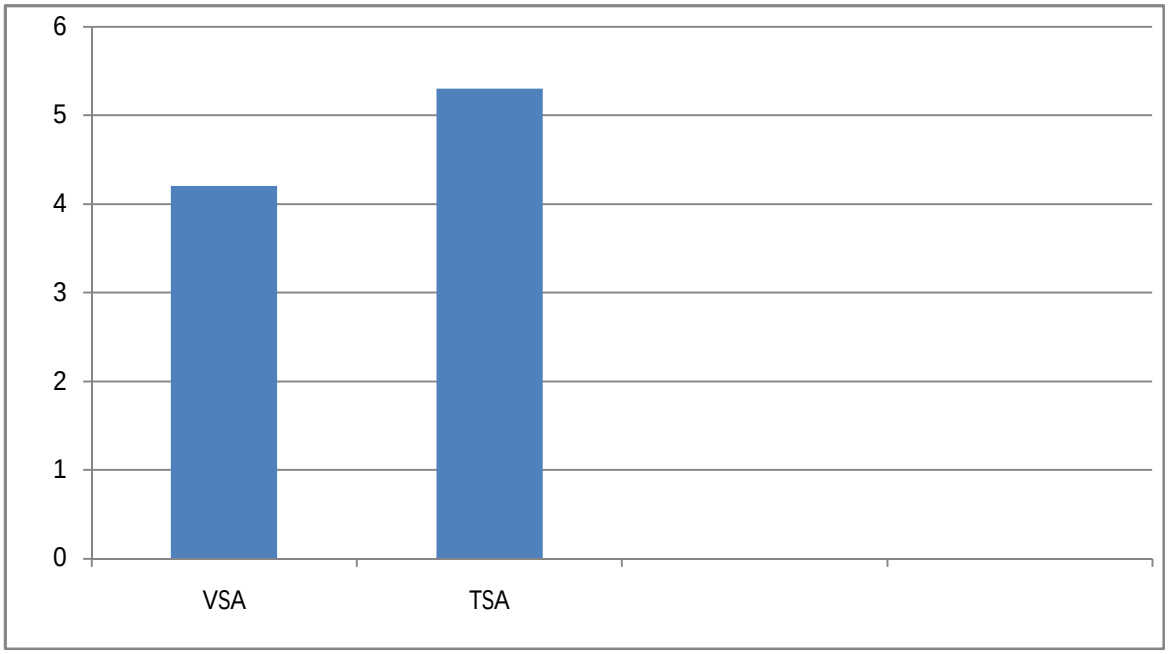

Fig7.Transistor Count between Voltage and Traditional Sense Amplifier

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BIOGRAPHY

Vucha bhandhavi is pursuing B.Tech in Electronics and Communication Engineering(E.C.E) from D.M.S.S.V.H College of Engineering, Machilipatnam, affiliated to Jawaharlal Nehru Technological University Kakinada. Areas of interest vlsi

S.Sridhar working as Assistant professor in Electronics and Communication Engineering (E.C.E) from D.M.S.S.V.H College of Engineering, Machilipatnam, affiliated to Jawaharlal Technological University Kakinada.

Mekala Ramya is pursuing B.Tech in Electronics and Communication Engineering (E.C.E) from College of Engineering Machilipatnam, affiliated to Jawaharlal Nehru Technological University Kakinada. Areas of interest vlsi

G.Mounika is pursuing B.Tech in Electronics and Communication Engineering (E.C.E) from D.M.S.S.V.H College of Engineering, Machilipatnam, affiliated to Jawaharlal Nehru Technological University Kakinada. Vlsi

T.Poojitha is pursuing B.Tech in Electronics and Communication Engineering (E.C.E) from D.M.S.S.V.H College of Engineering, Machilipatnam, affiliated to Jawaharlal Nehru Technological University Kakinada. Areas of interest vlsi

R.Mahesh Reddy is pursuing B.Tech in Electronics and Communication Engineering (E.C.E)from D.M.S.S.V.H College of Engineering, Machilipatnam, affiliated to Jawaharlal Nehru Technological University Kakinada. Areas of interest vlsi