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Design of Low-Power High-Performance 2-4 and 4-16 Mixed Logic Line Decoders

D Komali[1], S.Sridhar[2], J.Saibabu[3], B.Rohini Kumar[4], MD.Ameena[5]

B.Tech, Dept. of E.C.E, D.M.S.S.V.H College of Engineering, Machilipatnam, India[1345]

Assistant Professor, Dept. of E.C.E, D.M.S.S.V.H College of Engineering, Machilipatnam, India[2]

ABSTRACT: This paper introduces a mixed logic design method for line decoders, by combining pass transistor dual-value logic, transmission gate logic and static complementary metal-oxide semiconductor. Two new topologies are presented for the 2-4 decoder, a 14-transistor topology aiming on minimizing transistor count and power dissipation and a 15-transistor topology aiming on high power-delay performance. In each case both normal and inverting decoders are implemented, yielding a total of four new designs. Furthermore, by using mixed-logic 2-4 decoders combined with standard CMOS postdecoder, designed four new 4-16 decoders. All proposed decoders have full-swinging capability and reduced transistor count compared to their conventional CMOS counterparts. Finally, a variety of comparative EZ wave simulations at the 130nm (PYXIS GDK) shows that the proposed circuits present a significant improvement in power and delay, outperforming CMOS in almost all cases.

KEYWORDS: Line decoder, mixed-logic, power-delay optimization.

I. INTRODUCTION

Address decoder is essential elements in all SRAM memory block which respond to very high frequency. Access time and power consumption of memories is largely determined by decoder design. Design of a random access memory (RAM) is generally divided into two parts, the decoder, which is the circuitry from the address input to the word line, and the sense and column circuits, which includes the bit line to the data input/output circuits. Due to large amount of storage cells in memories it can be found various solutions of address decoder designs leading to power consumption reduction and performance improvement. Usually different kinds of pre charging dynamic decoders are used. Design of dynamic decoder is complex and having more probability of wrong sensing. Traditional static decoder gives more accurate result but it is having more number of transistors with large delay. Some solutions use hierarchical decoders with pre decoding and also implemented binary tree decoder built by De-multiplexers.

Decoders plays a crucial role in memory applications so we introduce high-speed a mixed-logic design method for line decoders.Address decoder using NAND-NOR alternate stages with pre decoder and replica inverter chain circuit is proposed and compared with traditional and universal block architecture, using 130nm CMOS technology. Delay and power dissipation is reduced in proposed design over existed design. Recently reported logic style comparisons based on full-adder circuits claimed complementary pass-transistor logic (CPL) to be much more power-efficient than complementary CMOS. High speed multiplier is implemented with the help of Complementary Pass transistor Logic (CPL) is a family of CMOS design. Same CPL technique is used to implement Arithmetic and Logic Unit [ALU] in for increasing the design speed. Transmission switch theory is introduced which is used for CMOS digital circuit design. Complex logic gate is implemented in based on pass transistor dual voltage logic for low power applications. Paper describes about develop a Karnaugh map based method that can be used to efficiently synthesize pass transistor logic circuits, which have balanced loads on true and complementary input signals. The method is applied to the generation of basic two-input and three-input logic gates in CPL, DPL and DVL. The method is general and can be extended to synthesize any pass-transistor network. Above papers describes different techniques to implement logic designs which gives better results in terms of area, delay and power consumption.

Three different decoder designs are implemented, they are AND–NOR, Sense–Amp, and the AND decoder. These pre charge based designs are analyzed the constraints (area, energy consumption and delay). AND based decoder

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has better energy consumption and delay than remaining designs. Novel design technique based decoder is implemented using 130nm CMOS technology which has better power consumption and delay compared with traditional decoder.

The proposed design is used mixed logic with the help of different techniques are observed from different existed logic circuits represented in above. Modified mixed logic decoder analysis increases the performance (delay and power) compared with existed CMOS NAND and NOR based decoder.The paper is divided as follows: Section II represents related work and designs. Section III represents proposed system. Section IV presents results and conclusion.

II. RELATED WORK

The authors used 20 transistors to design a 2-4 decoder and 104 transistors are used to design 4-16 decoders.

(a)2-4 decoder:

A 2-4 decoder has 2 inputs A and B and generates the 4 outputs D0-3.Based on the input combination, one of the four output is selected and set as 0, and the remaining are set as 1.A 2-4 decoder can be designed by using 2 inverters and 4 NOR gates, both yielding a total of 20 transistors and this can be shown in fig1(a).The truth table of the 2-4 decoder is shown in table 1.

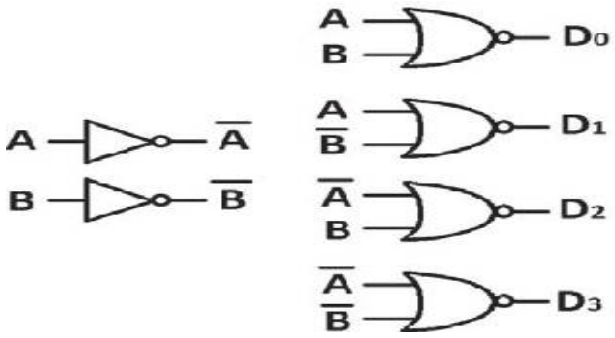

Fig 1(a): Non-Inverting 2-4 decoder

A	B	D_0	D_1	D_2	D_3
0	0	**1**	0	0	0
0	1	0	**1**	0	0
1	0	0	0	**1**	0
1	1	0	0	0	**1**

Table1: Truth table of 2-4 decoder

b) Inverting 2-4 decoder:

An inverting 2-4 decoder has 2 inputs A and B and generates the complementary outputs of I0-3.Based on the input combination one of the output is selected and set as 1 and the remaining are set as 0.An inverting 2-4 decoder can be designed by using 2 inverters and 4 NAND gates, both yielding a total of 20 transistors and this can be shown in fig 1(b).The truth table of the inverting 2-4 decoder is shown in table2.

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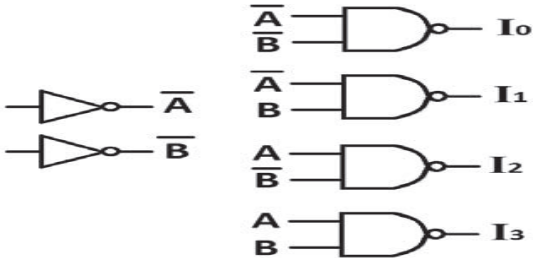


Fig 1(b): Inverting 2-4 decoder

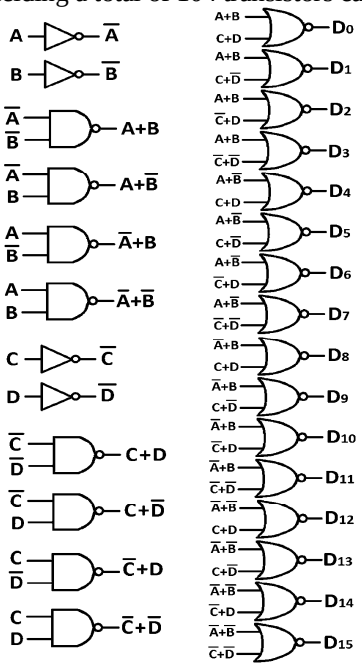
A	B	I_0	I_1	I_2	I_3
0	0	**0**	1	1	1
0	1	1	**0**	1	1
1	0	1	1	**0**	1
1	1	1	1	1	**0**

Table1: Truth table of 2-4 decoder

4-16 decoder:

A 4-16 decoder has 4 inputs A, B, C, D and generates the 16 outputs D0-15 and an inverting generates the complementary outputs I0-15.A 4-16 decoder can be designed by using 2 2-4 inverting decoders and 16 2-input NOR gates shown in fig2(a) whereas inverting 4-16 decoder can be designed by using 2 2-4 decoders and 16 2-input NAND gates shown in fig2(b), yielding a total of 104 transistors each.

(a)



(b)

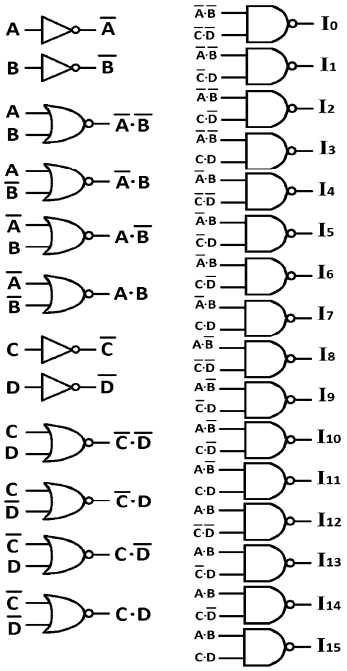


Fig 2(a): Non inverting 4-16 decoder Fig 2(b): Inverting 4-16 decoder

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III. PROPOSED SYSTEM

(a) 14-transistor 2-4 low power decoder:

A 14-transistor 2-4 low power can be designed by using either TGL or DVL gates would require 5 PMOS and 9 NMOS, whereas, 14 transistor inverting decoder would require 5 NMOS and 9 PMOS, yielding a total of 14 transistors each. The new 14 transistor 2-4 decoders are shown in fig 3(a) and fig 3 (b).

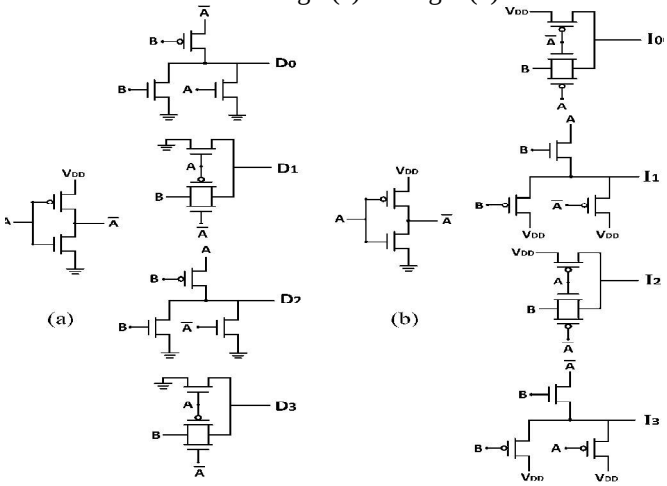

Fig (3): New 14 transistor 2-4 decoder (a) 2-4 LP (b)2-4 LPI

The D0 and D2 can be designed with DVL gates where A is used as the propagating signal and D1 and D3 can be designed with TGL gates in this B is used as the propagating signal, whereas in inverting I0 and I2 can be designed with TGL gates in this B as the propagating signal and I1 and I3 can be designed with DVL gates where B is used as propagating signal. The new two topologies are LP and LPI whereas LP stands as Low power and I as Inverter.

b) 15 transistor 2-4 High performance decoder:

The low-power topology presented above have a drawback in the case of D0 and I3 regarding worst case delay which comes from the use of complementary A used as the propagating signal. However, D0can be designed with CMOS NOR gate and I3 with CMOS NAND gate. The 2-4 HP can be designed by using 9nMOS and 6pMOS whereas 2-4HPI can be designed by using 6nMOS and 9pMOS, yielding a total of 15 transistors each. The 2-4HP and 2-4HPI decoders are shown in fig 4(a) and (b) respectively. So, in 15 transistors topology there is a improvement in delay compare than 2-4 low power topology but slightly increase in power dissipation.

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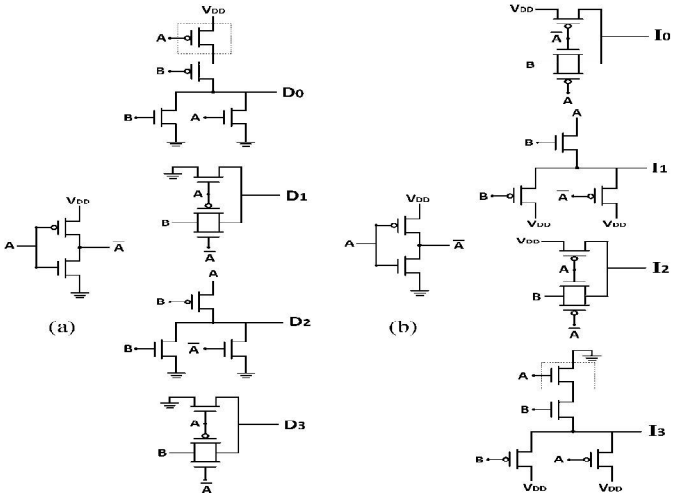

Fig(4) : New 15 transistor 2-4 decoder (a)2-4 HP (b)2-4 HPI

c) New 4-16 topology:

The 4-16 LP can be designed by combining 2 2-4LPI pre decoders with a NOR based post decoders shown in fig5(a) whereas 4-16LPI can be designed by combining 2 2-4LP pre decoders with a NAND based post decoder shown in fig5(b), yielding a total of 92 transistors. The 4-16HP can be designed by combining 2 2-4HPI pre decoders with a NOR based post decoders shown in fig5(c) whereas 4-16HPI can be designed by combining 2 2-4HP pre decoders with a NAND based post decoders shown in fig5(d), yielding a total of 96 transistors each.

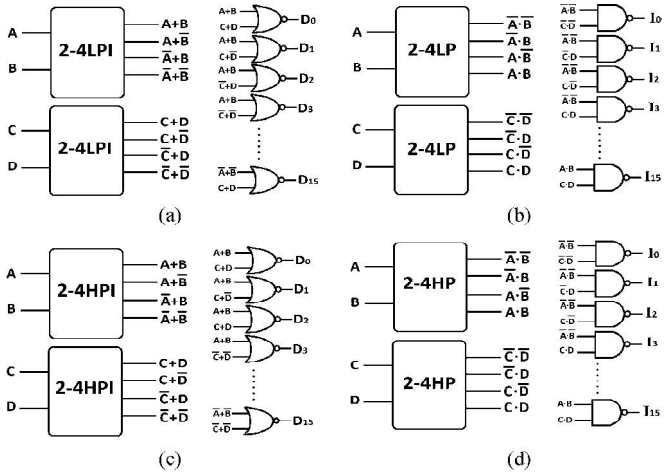

Fig 5 (a) 4-16LP (b) 4-16 LPI (c)4-16 HP (d)4-16HPI

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IV. SIMULATION RESULTS

Decoder designs are implemented using Mentor Graphics 130nm technology. Comparison results are represented in the table.

DELAY		
	2-4 Decoder	4-16 decoder
CMOS	46.373pS	85.252pS
LP	24.282pS	60.252pS
HP	6.2984pS	58.751pS
CMOS INV	20.874pS	158.15pS
LPI	11.838pS	79.026pS
HPI	5.2997pS	61.005pS

Table 3: Delay of decoders

Power Dissipation		
	2-4 decoder	4-16 decoder
CMOS	10.421nW	27.7020nW
LP	7.6282nW	21.5708nW
HP	7.6783nW	23.0905nW
CMOS INV	10.9182nW	42.4803nW
LPI	7.8527nW	36.9937nW
HPI	8.6125nW	36.9939nW

Table 4: Power dissipation of decoders

Power Delay Product(PDP)		
	2-4 decoder	4-16 decoder
CMOS	1039.2653Zj	20497.138zJ
LP	463.0820zJ	10958.45188zJ
HP	82.572zJ	10824.28424zJ
CMOS INV	509.8683zJ	43706.334zJ
LPI	113.7075zJ	16861.77762zJ
HPI	54.7512zJ	13116.075zJ

Table 5: Power_ Delay Product of decoders (PDP)

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Table 3 describes the delay of all decoders in which LP stands as low power, HP stands as high performance, LPI stands as low power inverter and HPI stands as high performance inverter. Table 4 describes the power dissipation of all decoders. Table 5 describes the power_delay product(PDP) of all decoders, it shows which one is better.

V. CONCLUSION

The simulation results showed that the proposed system compared with existed system. In this 2-4 LP decoders reduces power dissipation, delay and PDP by 26.3%, 47.6% and 55.4% over CMOS. 2-4 HP reduces power dissipation, delay and PDP by 26.32%, 86.4% and 92%. 2-4 LPI reduces power dissipation, delay and PDP by 28%, 43.2% and 77.6%. 2-4 HPI reduces power dissipation, delay and PDP by 21.1%, 74.6% and 89%. 4-16 LP reduces power dissipation, delay and PDP by 22.1%, 29.3% and 46.5%.4-16 HP reduces power dissipation, delay and PDP by 16.6%, 31% and 47.1% over CMOS. 4-16 LPI reduces power dissipation, delay and PDP by 12.9%, 50% and 61.4%. 4-16 HPI reduces power dissipation, delay and PDP by 12.9%, 61.4% and 69.9%.

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BIOGRAPHY

Dasari Komali is pursuing B.Tech in Electronics and Communication Engineering (E.C.E) from D.M.S.S.V.H College of Engineering, Machilipatnam, affiliated to Jawaharlal Nehru Technological University Kakinada. Areas of interest include VLSI.
S.Sridhar working as assistant professor in and Communication Engineering (E.C.E) from D.M.S.S.V.H College of Engineering, Machilipatnam, affiliated to Jawaharlal Nehru Technological University Kakinada.
Janyavula Saibabu is pursuing B.Tech in Electronics and Communication Engineering (E.C.E) from D.M.S.S.V.H College of Engineering, Machilipatnam, affiliated to Jawaharlal Nehru Technological University Kakinada. Areas of interest include VLSI.
Boddula Rohini kumar is pursuing B.Tech in Electronics and Communication Engineering (E.C.E) from D.M.S.S.V.H College of Engineering, Machilipatnam, affiliated to Jawaharlal Nehru Technological University Kakinada. Areas of interest include VLSI.
Mohmmed Ameena is pursuing B.Tech in Electronics and Communication Engineering (E.C.E) from D.M.S.S.V.H College of Engineering, Machilipatnam, affiliated to Jawaharlal Nehru Technological University Kakinada. Areas of interest include in VLSI.