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# Implementation of 9T SRAM Using Series Technique

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**ABSTRACT:** Inthis proposed method describes the various,techniques for low power VLSI circuits.This described paper focuses on leakage current in 9T transistor by series transistor combination technique. As power is proportional to Vdd, the power is reduced by 28.3%. There is a significant reduction of 36.3% of leakage current. The stability parameter SNM is calculated which shows that stability is increased by 10.9%. The static power is also reduced because of the stacking of PMOS and NMOS transistors. The parameters are calculated through TANNER EDA tool.

**KEYWORDS:** Optimization, sleep transistor, series transistors, SRAM

## I. INTRODUCTION

In the past decades, the main focus of VLSI designers were performance, area and design cost. Power consumption was most important relatively, and the use of memory in digital systems has been increased to a great extent. The advantage of utilizing combination of low-power design techniques in conjunction with low-power components is more valuable now. Heat pumped into the room, the electricity consumed and the office noise diminishes with low power VLSI chipset. To enhance the battery life of memory held devices, the consumption of power and power dissipation should be reduced.

## II. LITERATURE SURVEY

Overall, the proposed cell has less power dissipation than conventional cell due tostacking of PMOS, PMOS and NMOS transistors[1].Designing for low power adds another dimension to the already complex design problem; the design has to be optimized for Power as well as Performance and Area[2]. The results of 9T SRAM, we see that the read delay of this SRAM is high as nearly 1.45 higher than 6T SRAM‘s read delay[3].Different techniques have been analyzed to reduce the standby leakage current and dynamic power dissipation of the SRAM cell[4]. The energy consumption per read operation of the proposed SRAM cell is much lower than those of the previous SRAM cells thanks to the elimination of unnecessary BL discharge through the use of a column-based VVSS[5]. A 16Kb (256×64) 28nm FDSOI 9T SRAM test chip demonstrates that the proposed CS-CVSS scheme with DAWA achieve 390 mV lower VDDMIN-Write than 8T SRAM without write assist[6].The proposed circuit with the basic design same as 6T SRAM cell, have footer transistor leads to the reduction ofthe static power[7].

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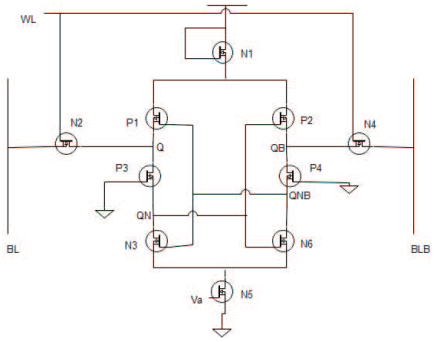
I.SLEEP TRANSISTOR mode:




Block diagram

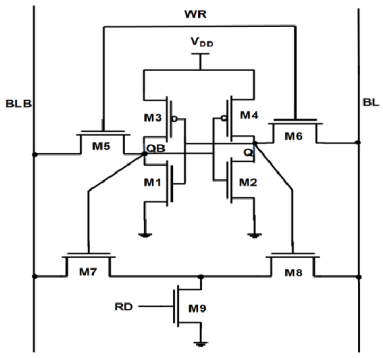
A. *Read operation:*

While reading '1'Q is at '1' and QN is at'1' (since P3 is always on state.) so QnB is at '0'. Since BLB is pre-charged so this might cause the flipping. of the contents of the storage nodes. To avoid this, P4 which is always in ON state, is added, When WL is enabled, the voltage gets divided across N4, P4, and NM6 in series. This suppresses rising of QNB voltage to VDD - VTN4 - |VTP4| where VTN4 is threshold voltage of N4 and VTP4 is threshold voltage of P4.

*B. Write Operation:*

While writing '0' QN is at '1'and QNB is at '0', so Q changes its state from '1' to '0' and QNB gets discharged to state zero Due to stacking of PMOS, PMOS and NMOS transistors in the proposed 9T SRAM,(with sleep transistor) cell, the static power dissipation is reduced. The purpose of adding NMOS5 transistor as sleep transistor is to reduce the leakage current.

## II. SERIES TRANSISTOR TECHNIQUE




Block Diagram:

A. *Read Operation:*

uring a read operation, RD signal transitions high while WR is maintained low, as illustrated in Fig. 2(b). The read access transistor N7 is activated. Provided that Node1 stores "1" [as assumed in Fig. 2(b)], BL is discharged through N5 and N7. Alternatively, provided that Node2 stores "1", the complementary bitline (BLB) is discharged through N6 and N7 uring a read operation, RD signal transitions high while WR is maintained low, as illustrated in Fig. 2(b). The read access transistor N7 is activated. Provided that Node1 stores "1" [as assumed in Fig. 2(b)], BL is discharged through N5 and N7. Alternatively, provided that Node2 stores "1", the complementary bitline (BLB) is discharged

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through N6 and N7 During a read operation, RD signal transitions high while WR is maintained low, as illustrated in Fig. 2(b). The read access transistor N7 is activated. Provided that Node1 stores “1” [as assumed in Fig. 2(b)], BL is discharged through N5 and N7. Alternatively, provided that Node2 stores “1”, the complementary bitline (BLB) is discharged through N6 and N7 A Read operation, RD signal transitions high while WR maintained low. The read access tran- sistor N7 is activated. Provided that Node1 stores "1"BL is discharged through N5 and N7. Alternatively, provided that Node2 stores "1", the complementary bitline (BLB) is discharged through N6 and N7.

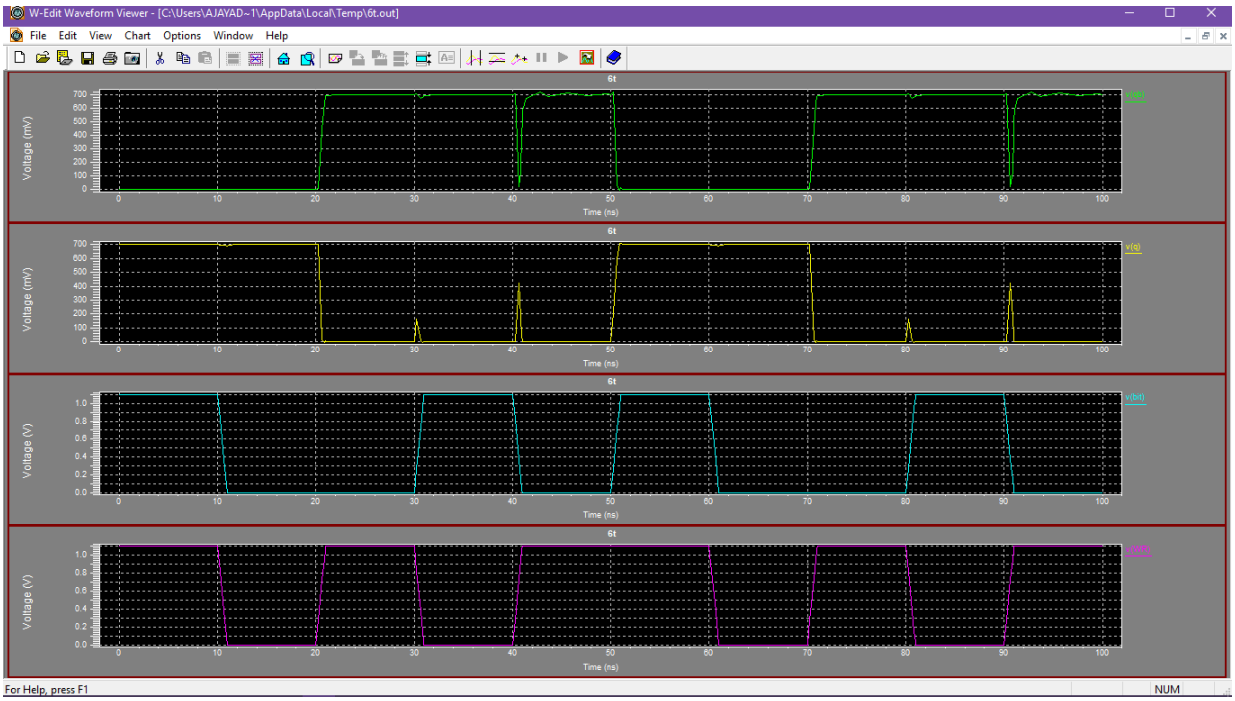
B. Write Operation:

A Write operation, WR signal transitions high while RD is maintained low, as sh N7 is cutoff. The two write ac- cess transistors N3 and N4 are turned on. In order to write a "0" to Node1, BL and BLB are discharged and charged, respectively. A "0" is forced into the SRAM cell through N3. Alternatively, for writing a "0" to Node2, BL and BLB are charged and discharged, respectively.

## III. RESULTS AND SIMULATIONS

All the circuits have been simulated using BSIM 3V3 140nm technology on Tanner EDA tool with supply voltage ranging of (.7v). The basic SRAM structure can be significantly optimized to minimize the delay and power at the cost of some area overhead. The optimization starts with the design and layout of the RAM cell, which is undertaken in consultation with the process technologists. For the most part, the thesis assumes that a ram cell has been adequately designed and looks at how to put the cells together efficiently. The power results values are calculated at different supply voltages and frequency. In our proposed memory design consume less power compared to design a 9T SRAM sleep transistor cell.

Simulation Results:-




Sleep Transistor results.
VoltageSource. v1

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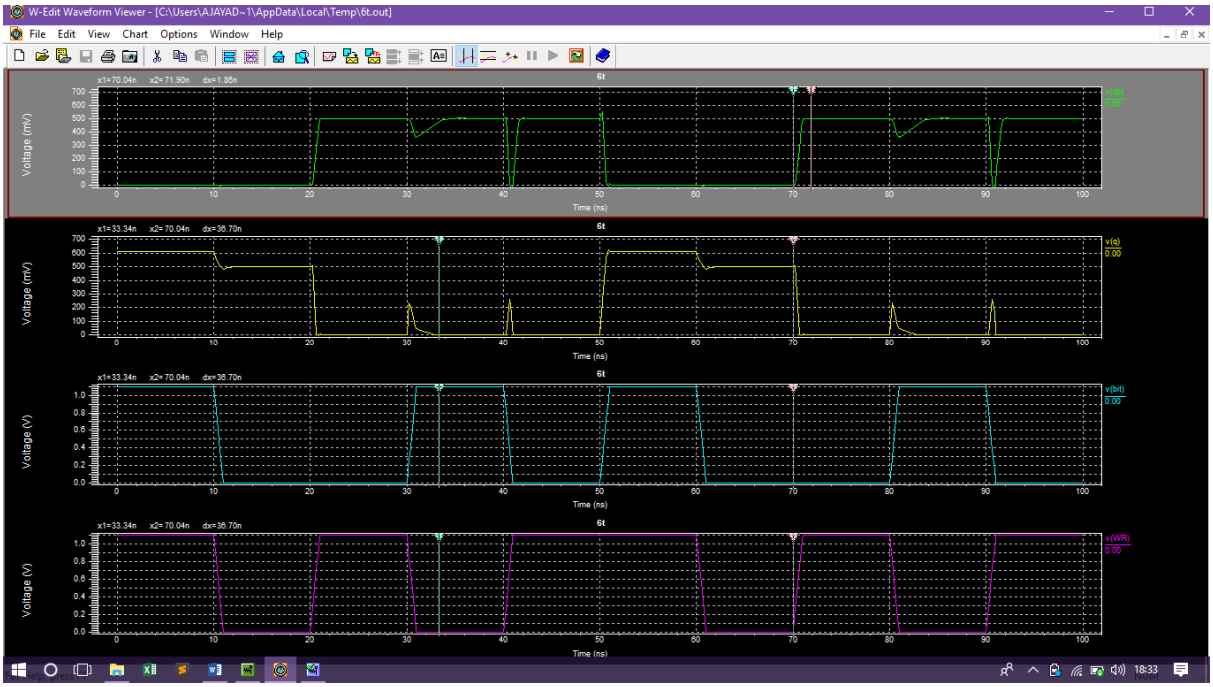
VOLTAGE 1.10000 1.10000
CURRENT LEAKAGE-118.86649n
POWER -130.75314n 0
TEMP [27 C]
Now whereas the proposed models results are calculated and shown.
Simulation for Series Method.




VOLTAGE 1.10000 1.10000 500.00000m
CURRENT -1.80439u 0. 1.80436u
POWER -1.98483u 0. 902.17938n
TEMP [27 C]
Average power consumed -> 6.466906e-008 watts
Max power 1.282761e-005 at time 9.1e-008
Min power 1.203581e-010 at time 3.86619e-008

| Delay | |
|---|---|
| SLEEP TRANSISTOR TECHNNIQUE | 3.75n |
| SERIES TRANSISTOR TECHNNIQUE | 1.35n |

## IV. CONCLUSION

In this paper 9T SRAM with sleep transistor is presented to reduce average power dissipation and stability.The results are calculated at 35nM.CMOS technology for different supply voltages (0.6v,0.7v,0.8v)and then compared to conventional 9T SRAM.Average powerdissipation was reduced by 28.3%.Static power dissipation was reduced by10.9% and leakage current was reduced by 36.3%.In addition to these parameters SNM was also calculated.There was an increase SNM by 98.2% which is power dissipation is significant for stability. Overall the proposed cell has less

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power dissipation than conventional cell due to stacking of PMOS, PMOS and NMOS transistors.Even though the presented cell,it is not a concern since 9T SRAM with sleep transistor cannot give stable values at low voltage unless cell ratio and pull up ratio are increased which in turn increases transistor count and thus area is increased.

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