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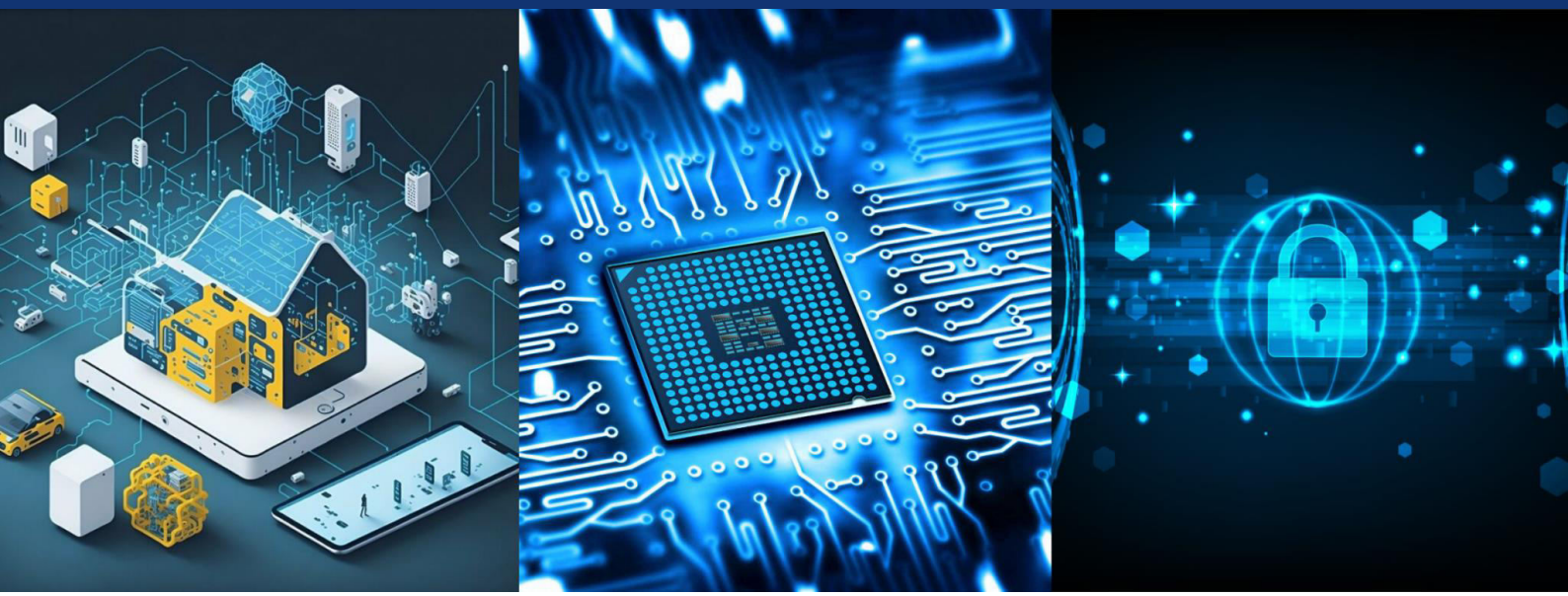

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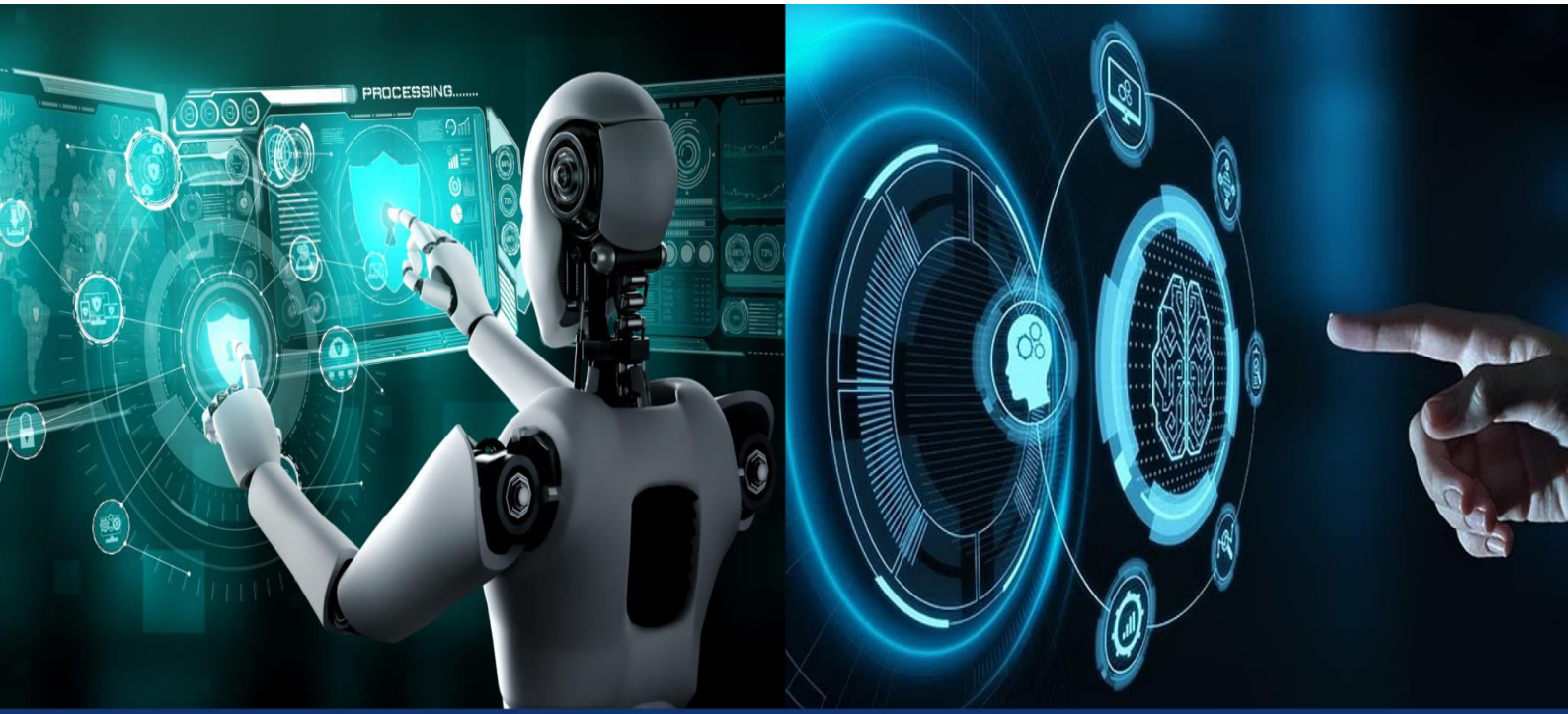

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Optimized Fault-Tolerant Linear Feedback Shift Register for Low Power Applications

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ABSTRACT: VLSI aims to integrate thousands of transistors onto a single chip for better area utilization and interconnection efficiency. Linear Feedback Shift Registers (LFSRs) are commonly used for generating pseudo-random sequences and find applications in random number generation, fast counters, and BIST systems. However, traditional LFSRs are prone to Single-Point Failures (SPoFs), where one fault can disrupt the system.To improve reliability, a Fault-Tolerant LFSR (FT-LFSR) using enhanced Triple Modular Redundancy (TMR) is proposed. This method uses three identical modules and majority voting to maintain correct functionality, even in the presence of faults. Flip-flop clock gating is also applied to reduce power consumption by disabling inactive circuit parts.Experimental results using Xilinx tools show that the FT-LFSR is effective against most fault types while maintaining low power, making it suitable for reliable and energy-efficient VLSI systems.

KEYWORDS: LFSR, VLSI, FT-LFSR, TMR, Clock Gating, Xilinx Vivado Software.

I. INTRODUCTION

Recent advancements in high-speed counter design have drawn significant attention due to their importance in wide bit-width applications, including frequency synthesizers, phase-locked loops (PLLs), analog-to-digital converters (ADCs), and time-to-digital converters (TDCs). These systems demand not only precision but also rapid counting capabilities across large data ranges. However, traditional binary counters face limitations when scaling up to meet these demands. As the bit-width increases, the complexity and delay in synchronous binary counters—especially those using adders and state registers—also increase, making it difficult to maintain a constant and high clock frequency.

In conventional designs, the delay associated with the adder grows with the counter size, directly impacting performance. As a result, such counters become inefficient for high-speed applications. To overcome these challenges, alternative architectures are being explored—most notably the use of Linear Feedback Shift Registers (LFSRs).

LFSRs are known for their ability to generate pseudo-random sequences with minimal hardware. They consist mainly of D flip-flops and XOR gates and can be designed to operate at a fixed delay irrespective of the bit-width. Their constant-time behavior makes them an excellent candidate for high-speed and low-complexity counters. Unlike binary counters, where each state is a linear increment from the previous, LFSRs transition through a sequence of states determined by a feedback polynomial, allowing for faster and more efficient counting in some contexts.

LFSRs can be broadly categorized into two feedback configurations:
Many-to-One LFSR: Multiple flip-flops contribute to a single feedback input. This structure closely resembles a traditional binary counter and typically provides better randomness but may operate slower due to multiple inputs affecting feedback delay.

One-to-Many LFSR: A single flip-flop output is distributed to multiple feedback paths. This setup tends to be faster but may offer reduced sequence complexity.Historically, many implementations have favored the many-to-one LFSR structure, using it as a direct replacement for binary counters without fully exploring its speed trade-offs. For instance, digital CMOS image sensors have adopted LFSR-based counters for analog-to-digital conversion to achieve faster

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operation with fewer components. Similarly, ring oscillator-based physically uncloneable functions (PUFs) employ many-to-one LFSRs to generate unique pseudo-random patterns critical for security.

In time-of-flight (ToF) camera systems, multistage LFSR counters have also been introduced to handle rapid pixel data conversion. These systems benefit from the simplicity and speed of LFSRs but face a fundamental limitation: an m-bit LFSR only covers 2^m - 1 states, unlike a full binary counter that covers all 2^m states. Therefore, additional logic is required to extend the state space and map the LFSR outputs to equivalent binary values.

This state extension must be tightly synchronized with the LFSR's operation to prevent loss of performance or accuracy. Some approaches attempt to solve this via lookup tables (LUTs) or iterative decoding, but each method has trade-offs. reduce memory usage but add latency, leading to a classic time-memory trade-off.

A multistage Linear Feedback Shift Register (LFSR) counter architecture has been introduced to address concerns related to complexity and performance. By connecting multiple LFSRs in sequential stages, each stage contributes to a portion of the final output.

This configuration reduces the complexity of individual LFSRs and distributes the processing load across stages, potentially enhancing scalability and overall performanceDespite their advantages, LFSRs still require careful design to ensure consistent timing, state coverage, and reliable binary translation. Researchers continue to explore hybrid solutions combining LFSRs with other counter types or error detection/correction mechanisms to further enhance their utility in modern high-speed VLSI systems.

II.RELATED WORK

Many communication systems and cryptographic applications require circuits with minimal delay, lower area, and efficient power consumption. As discussed in earlier sections, Linear Feedback Shift Registers (LFSRs) are widely used in applications such as cyclic redundancy check (CRC) generation, cryptography, and pseudorandom number generation, where speed and compact design are essential.
In 2004, K.K. Parhi proposed a technique to eliminate the fanout bottleneck in parallel long BCH encoders [1]. The study introduced efficient designs that distribute the fanout loads, thereby reducing critical path delay and achieving high-speed performance, essential for high-throughput encoders. This architecture improved speed without compromising on area or power significantly.

Later in 2009, C. Kennedy and A. Reyhani-Masoleh designed improved high-speed CRC computation techniques based on state-space transformations [2]. Their approach minimized the critical path by optimizing the computation of CRC residues, making the system more suitable for high-speed data transmission with reduced hardware complexity.
Building upon the need for fast feedback architectures, M. Ayinala and K.K. Parhi in 2010 proposed an efficient parallel VLSI architecture for LFSRs [3]. Their design was based on parallel processing of LFSR stages to significantly decrease delay, enabling faster throughput compared to conventional serial LFSR designs.

Extending this work, in 2011, Ayinala and Parhi developed high-speed parallel architectures specifically targeting LFSRs [4]. Their approach utilized optimized parallelization strategies and feedback computations, allowing for flexible parallelism degrees while maintaining a minimal critical path, thus boosting the operational frequency without large area overhead.

In 2012, D. Muthiah and A.A.B. Raj implemented a high-speed LFSR design using parallel architectures [5]. Their methodology focused on achieving speed improvements with careful trade-offs between area and power consumption, particularly suitable for communication systems requiring fast pseudorandom sequences.

Further advancements were made in 2015 by J. Jung, H. Yoo, Y. Lee, and I.C. Park, who proposed an even more efficient parallel architecture for LFSRs [6]. Their design minimized hardware complexity while maximizing processing speed through novel rearrangements of LFSR feedback paths, offering enhanced energy efficiency and better scalability for integration into modern high-speed applications.

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The evolution of these parallel architectures demonstrates a consistent drive toward achieving circuits with reduced delay, lower area, and optimized power usage, especially for applications requiring fast, secure, and reliable data processing. With the integration of high-speed LFSR and CRC computation techniques, modern processors and communication modules can achieve better performance without significantly increasing resource utilization.

III. EXISTING METHOD

Existing LFSR (Linear Feedback Shift Register) methods primarily rely on serial architectures that use chains of D flip-flops and XOR gates to generate pseudo-random sequences, but these suffer from limited speed and increased delay as bit-width increases. To overcome these issues, various parallel architectures have been proposed.

Parhi (2004) addressed the fanout bottleneck in BCH encoders, while Kennedy and Reyhani-Masoleh (2009) introduced high-speed CRC computation using state-space transformations. Ayinala and Parhi (2010, 2011) extended this by proposing efficient parallel LFSR architectures using transformation matrices to generate multiple bits per cycle.

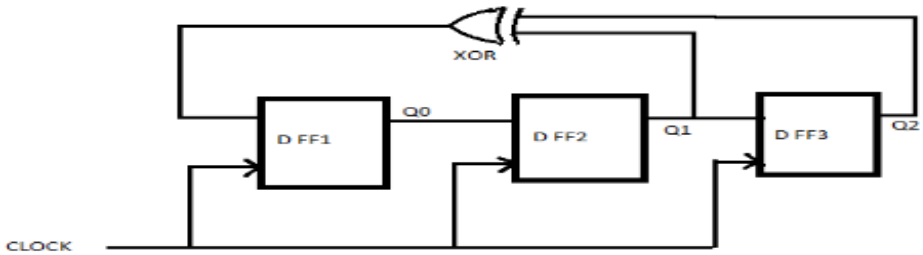

Fig.1: Linear Feedback Shift Register

Later works by Muthiah and Raj (2012), Jung et al. (2015), and Hu et al. (2017) focused on further optimizing delay and hardware efficiency using improved feedback logic and state-space strategies.
These designs commonly use many-to-one or one-to-many feedback configurations to manage propagation delay, though challenges like limited scalability, difficulty in binary state conversion, fan-out complexity, and synchronous state extension remain in conventional designs.

IV. PROPOSED METHOD

Traditional fault tolerant LFSRs include large number of Single-Point-ofFailures (SPoFs) in which any fault results in the whole system failure. In this proposed technique, a new fault tolerant architecture for LFSR (named as FT-LFSR) is proposed in which the number of SPoFs are significantly reduced compared to the previous ones. To this end, a modified version of Triple Modular Redundancy (TMR) empowered with some extra controlling units for identifying the operational module is used. The proposed approach shows, concept of reducing the transitions in test pattern generated. The transition is reduced by increasing correlation between the successive bits. The simulation results shows how patterns are generated for the applied seed vector.

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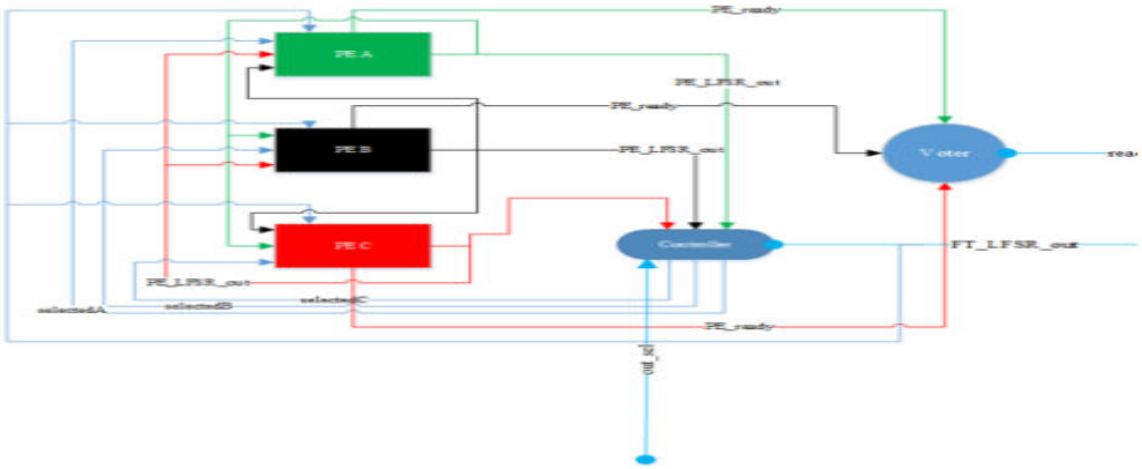

Fig. 2. Block diagram of proposed FT-LFSR

The proposed architecture FT-LFSR has three PEs and one voter based on TMR approach with Controller module which reduces the number of SPoFs.

This architecture has two outputs and one input:
1. outsell: out_sel comes from a module which controls the FTLFSR (e.g. BIST) and determines which PE must be connected to FT LFSR out (selected PE).
2. FT LFSR out: FT LFSR out is the N bit output of selected PE which is the same as a conventional LFSR's output.
3. FT LFSR out: FT LFSR out is the N bit output of selected PE which is the same as a conventional LFSR's output.
4. ready: ready shows that FT LFSR out is valid or not. if ready equals one, it means that FT LFSR out is valid and otherwise it means invalid. To demonstrate how this FT-LFSR works from when input is given until two outputs are ready, the following steps are done respectively:
• PE corresponds to Processing Element. Each PE is a conventional LFSR. • The second and third items clock and reset are also the inputs of FT-LFSR but they are not shown in the figure to not make it messy. At first, out_sel which is a 2-bit input for Controller, is initialized. Then Controller decides which PE LFSR out must be connected to FT-LFSR out. Now FT-LFSR out is available. This output goes to PEs to compare. Controller signals which PE is selected PE by selected A, selected B and selected C. Each PE based on being selected or not determines to compare its output with whom. Selected PE compares its output with two other PE's outputs and other PEs compare their outputs just with FT-LFSR out (selected PE's output). After comparison, each PE produces PE ready that shows correctness of FT-LFSR out based on its point of view. If no mismatch in total N bits occurs then PE ready=1, otherwise PE ready = 0. Finally, Voter which is a majority voter, votes between PE readys of PE A, PE B and PE C and sets/resets the ready output. Now one period of FT-LFSR is finished.

I.CLOCK GATING:
Reduction in power dissipation is an essential design issue in VLSI circuit. Few decades back designers mostly focus on area, delay and testability to optimize. While technology scaling down, we can see more power leakage and dissipation in chip. In order to reduce power dissipation and leakage power while scaling, we need to adopt the optimize techniques like clock gating, voltage scaling etc.
If operations are more and more complex then power dissipation is more. The clock network is a major source of power dissipation so we can reduce significant amount of power if we can gate the clock whenever it isn't required.
In our proposed work, we mainly focused on dynamic power dissipation and it reduced by making less signal activities in proposed design. The clock network is a major source of power dissipation so we can reduce significant amount of power if we can gate the clock whenever it isn't required.

II.FLIPFLOP_BASED CLOCKGATING:
In many applications, latch based designs are moved to flip flop based designs. By splitting flip flop, we can see twolatches from the master slave theorem. In this technique, we can see D flip flop with AND gate.

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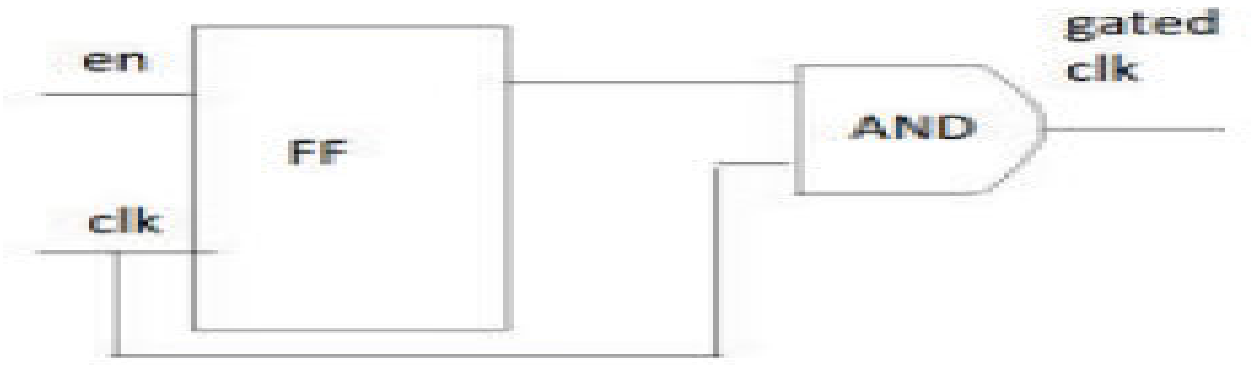

Fig. 3. FLIPFLOP_BASED CLOCKGATING

From the above figure, gated clock goes to high when flip flop output and clock are in high state otherwise gated clock goes to zero state. That means when clock in sleep mode then gated clock also in zero

From the above figure, gated clock goes to high when flip flop output and clock are in high state otherwise gated clock goes to zero state. That means when clock in sleep mode then gated clock also in zero state.

V. RESULTS

RTL schematic: The RTL diagram shows a two-level LFSR whose flip-flops and XOR taps are triplicated with majority voters, ensuring the pseudo-random sequence stays correct even if a bit fault occurs.

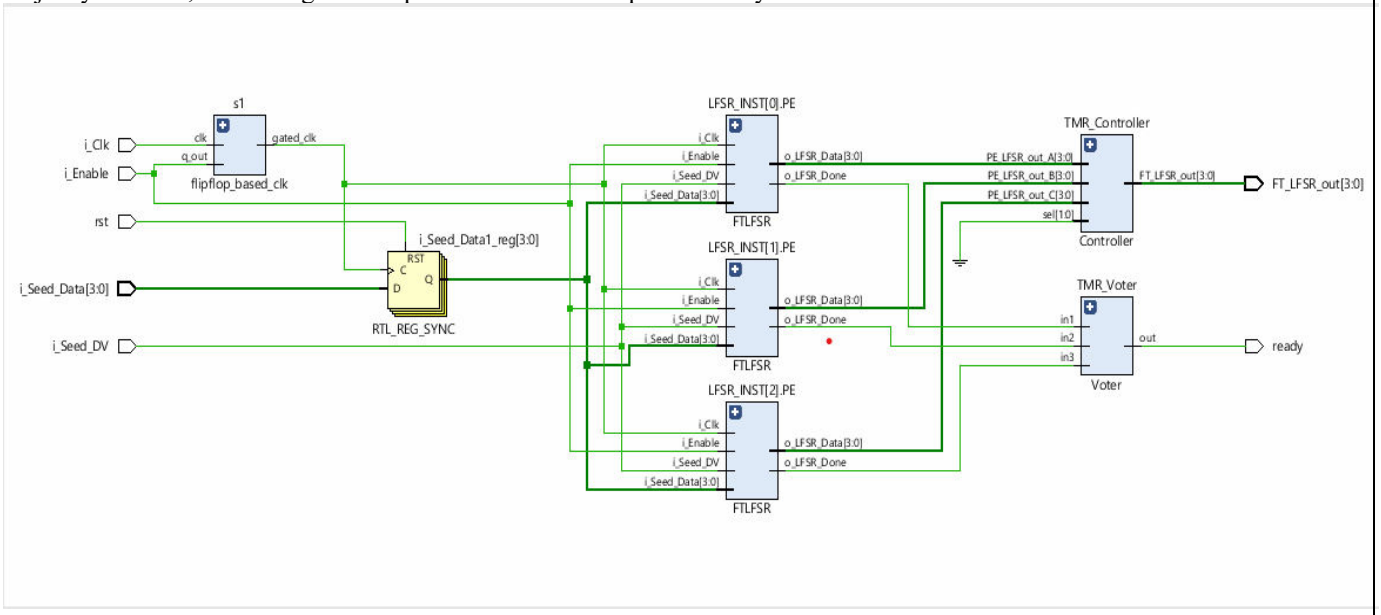

Fig. 4.: RTL Schematic for Proposed FTLFSR

Simulation Waveform: The simulation waveform displays synchronized clock pulses, triplicated state-bit streams, and aligned majority-voted outputs, confirming the proposed fault-tolerant two-level LFSR continuously produces an error-free pseudorandom sequence despite injected bit upsets.

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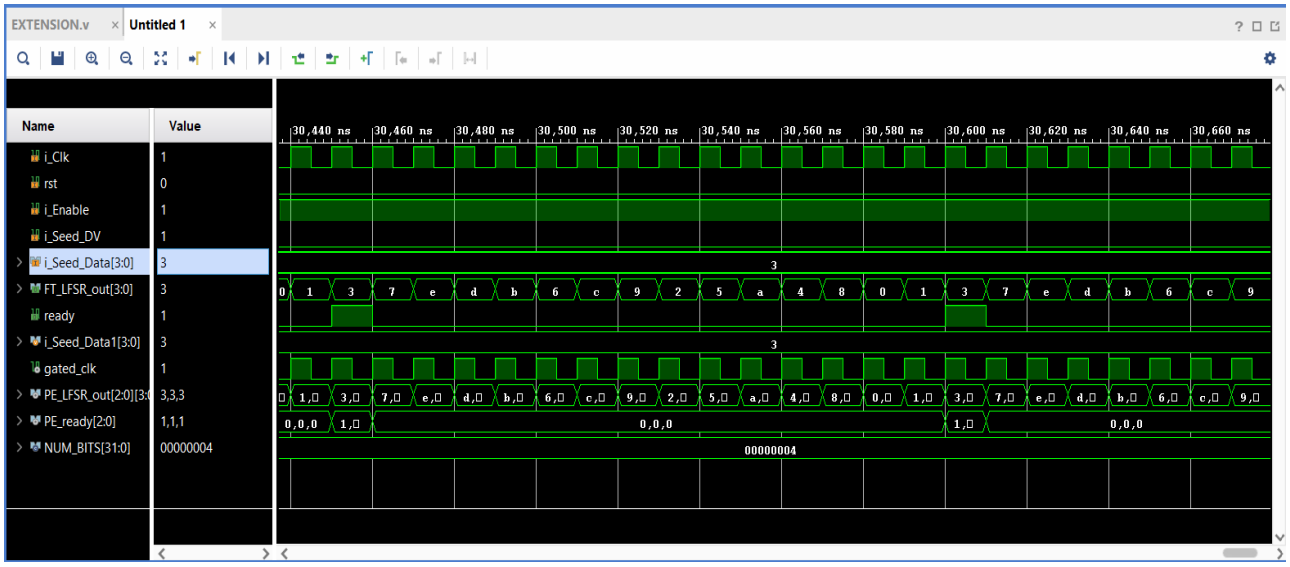

Fig. 5. Simulation Waveform for Proposed FTLFSR

Area: The proposed FTLFSR's fault-tolerance is achieved by triplicating the LFSR logic and adding compact voter/parity blocks, so its silicon/LUT footprint grows from the base design to roughly threefold plus a minimal control overhead.

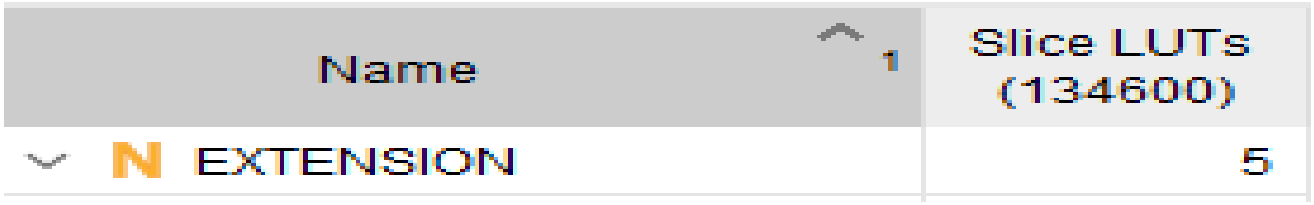

Fig. 6. Area for Proposed FT-LFSR

Delay: The critical-path delay increases slightly versus the baseline LFSR because the majority-voter (or parity-check) gates sit after the XOR feedback network, but overall latency remains dominated by a single XOR depth, keeping the design clock-friendly.

Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay
Path 1	∞	4	4	3	LFSR_INST[0]...SR_reg[1]/C	ready	4.901

Fig.7: Delay for Proposed FT-LFSR

Power: The power for the proposed FTLFSR (Feedback with Tapped Linear Feedback Shift Register) is primarily determined by the hardware implementation, with factors like clock frequency, bit width, and the logic gates used in the design affecting overall power consumption.

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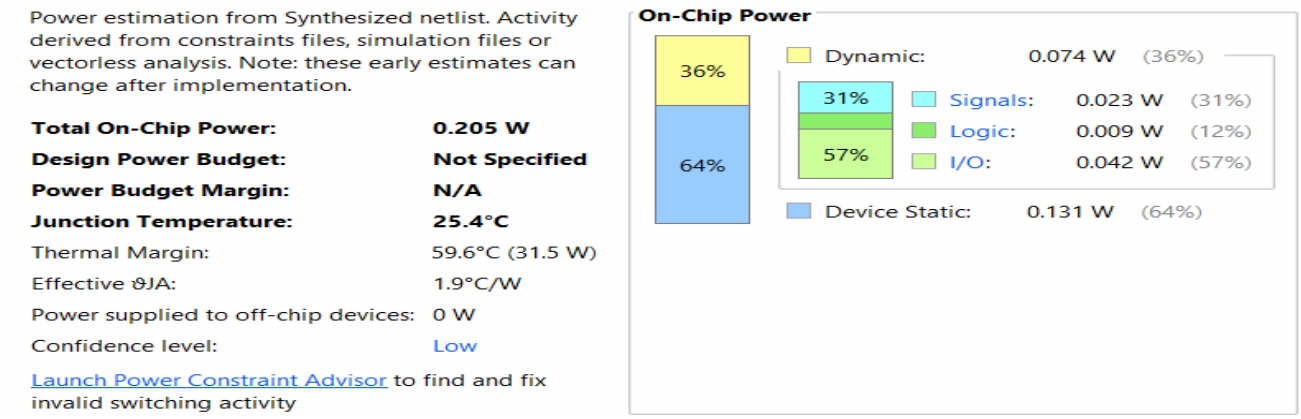

Fig. 8. Power for Proposed FTLFSR

Comparison Table:

	Area (LUT's)	Power(W)	Delay(nS)
FTLFSR	**4**	**2.292**	**5.090**
Proposed	**5**	**0.205**	**4.901**

VII. CONCLUSION

By applying flip-flop-based clock gating, power consumption in the Fault-Tolerant LFSR (FT-LFSR) with Triple Modular Redundancy (TMR) can be further reduced.

This approach enhances reliability and energy efficiency in LFSR-based applications such as BIST, CRC, and pseudorandom sequence generation. By mitigating Single Points of Failure (SPoFs) and minimizing unnecessary transitions through correlated test patterns, the architecture not only improves fault tolerance but also optimizes power usage. Additionally, the integration of clock gating ensures that only the necessary parts of the circuit are active during operation, reducing dynamic power dissipation. Simulation results validate the design's robustness, making it a highly efficient solution for error-resilient, low-power VLSI applications. This optimization ensures that the FT-LFSR with TMR can operate effectively in power-constrained environments without compromising on fault tolerance or performance.

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