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Offset Reduction of CMOS Based Dynamic Comparator by using Charge Storage Techniques - A Comparative Study

Neerav Mehan[1], Anshul Kumar[2], Kamna Kohli[3], Neha Sharma[4]

Assistant Professor, Dept of E.C.E, BUEST, Baddi, Solan (Dist), Himachal Pradesh, India[1,2,4]

Lecturer, Dept of E.C.E, BUEST, Baddi, Solan (Dist), Himachal Pradesh, India[3]

ABSTRACT: Comparator is one of the most widely used building block for analog and mixed signal systems. For the implementation of high-performance CMOS A/D converters, low offset comparators are essential. In this paper, dynamic comparator offset is calculated to the extent of high accuracy. The offset so calculated has been reduced by the charge storage techniques to achieve an efficient design. In addition to the offset, propagation delay and power dissipation, being the important parameter of the comparator, has been analyzed. It is observed that offset voltage in the comparator has been reduced to 350µV for output offset storage technique and 400µV for input offset storage techniques from 91mV. In this paper, BPTM model has been used in analyze the dynamic comparator.

Keywords- Dynamic comparator, offset voltage, storage capacitor, input offset storage, output offset storage.

I. INTRODUCTION

A comparator is essential component of an ADC. A comparator compares a differential input signal with a predetermined threshold voltage and gives a digital decision accordingly [1]. The major portion of the total power consumption results from the static power dissipated in analog circuit components that require DC bias currents. One efficient method is to use a dynamic comparator. In this way the static power consumption can be reduced. But at the expense of high offset error. Because such comparator topologies do not have static pre-amplification in the front of a latch part, thus have unavoidably large offset voltages.

The offset of a comparator can be defined by additional differential input signal to the ideal differential input to achieve a desired output [2]. Offset voltage affects the accuracy of the circuit. In order to achieve an optimum comparator design, it is essential to have accurate methods to predict offset voltages.

In this work, Section 2 describes the brief introduction about preamplifier based dynamic comparator. Section 3 presents the offset voltage minimization techniques. Section 4 deals with the results and discussions. Finally the section 5 offers the brief conclusion.

II. PREAMPLIFIER BASED DYNAMIC CMOS COMPARATOR

Device mismatch results in an input referred offset for the latch as a result of threshold voltage, W/L, and μC_{ox} variations [3]. Therefore, the latch must be preceded by a circuit that amplifies the (V_{IN} - V_{REF}) difference before it is applied to the latch. This amplifier circuit must have a large enough gain so that the minimum difference signal to be resolved is amplified to a voltage large enough to overcome the input referred offset of the latch [4].

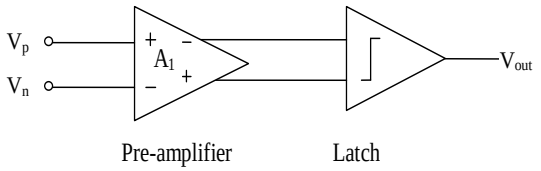

Fig. 1 Block diagram of pre-amplifier based dynamic comparator

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Fig. 1 shows the block diagram of a pre-amplifier based dynamic CMOS comparator. It consists of the two stages viz. pre-amplifier and latch. Preamplifier circuit is a differential amplifier with active loads. The output currents of the preamplifier are mirrored into the latch stage. The latch stage consists of a cross-coupled pair of NMOS and PMOS transistors.
In this preamplifier based comparator circuit offset is stored and canceled without adding any extra timing overhead by using input offset storage (IOS) and output offset storage (OOS) techniques.

III. OFFSET CANCELLATION TECHNIQUES

The analog sampling capability inherent in CMOS and BICMOS technologies provides a means whereby offsets can be periodically sensed, stored, and then subtracted from the input [5]. Both of the offset cancellation topologies i.e. IOS and OOS comprise a preamplifier, offset storage capacitor, and a regenerative latch. With IOS, the cancellation is performed by closing a unity-gain loop around the preamplifier and storing the offset on the input coupling capacitors. With OOS, the offset is cancelled by shorting the preamplifier inputs and storing the amplified offset on the output coupling capacitors. Both circuits are driven by a clock. The two-phase non overlapping clocking used to operate the circuits.

A. Input offset storage (IOS)

Fig. 2 shows the application of input offset storage (IOS) technique to the dynamic comparator consists of a preamplifier, offset storage capacitors (C_s) and a latched comparator. C_p is the parasitic capacitance at each charge observation node, which includes the input capacitance of the pre-amplifier, parasitic capacitance at the drain of the transistors in switches S_{3a}/S_{3b}, and the capacitance of the metal interconnects.

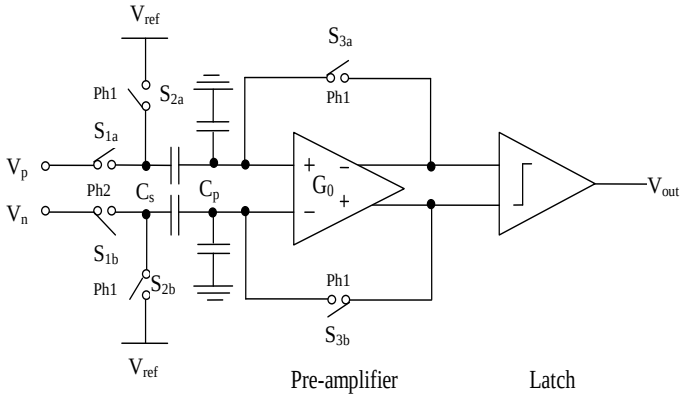

Fig. 2 Input offset storage technique

The comparator examines the input in ph2 – normal operation. Reference voltages are applied to the capacitors during ph1 which is the offset sampling phase. During this phase, the switches $S_{2a}/S_{2b}/S_{3a}/S_{3b}$ turn on, resettling the input and closing a unity gain loop around the preamplifier. In this situation its differential input voltage,

$$v_{IA} = \frac{G_o V_{OSa}}{1+G_o} \qquad (1)$$

is stored on the capacitor. In eq. (1) G_o is the DC gain of the preamplifier, and V_{OSa} is its offset voltage. G_o approaches V_{OSa} for high gain.
Capacitors are connected to the input signal during phase ph2. Capacitors in this phase provide the subtraction between the input, the reference voltages, and v_{IA}. Then preamplifier performs the amplification.
When a MOS transistor is turned off, the charges in its conducting channel are released and removed through the MOS source and drain terminals. In this way when S_{3a}/S_{3b} opens their transistors inject a certain amount of charge into the capacitors. The mismatches between S_{3a} and S_{3b} cause a difference Δq in the injected charges into the capacitor C_s.

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Therefore disturbing the differential voltage sampled in C_s. The introduction of the offset storage capacitors actually increase the contribution of offset voltage V_{osl}.
The total residual offset is (i.e. the offset after calibration) is

$$V_{OS} = \left(1 + \frac{C_P}{C_S}\right)\left[\frac{V_{OSa}}{1+G_O} + \frac{V_{OSl}}{G_o}\right] + \frac{\Delta q}{C_S} \qquad (2)$$

The offset can be minimized by enlarging the gain of the pre-amplifier, G_o, but this reduces its settling period. It is also important to make C_s significantly larger than C_p to decrease the C_p/C_s term.

B. Output Offset Storage (OOS)
Fig. 3 shows the application of output offset storage (OOS) technique to the dynamic comparator consists of a preamplifier, offset storage capacitors C_s, and a latched comparator.

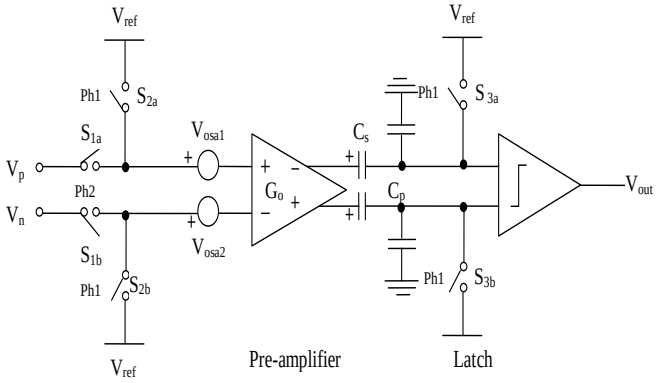

Fig. 3 Output offset storage technique

Offset sampling phase is ph1, where switches $S_{2a}/S_{2b}/S_{3a}/S_{3b}$ turns on. S_{2a}/S_{2b} and S_{3a}/S_{3b} force, respectively, a zero differential voltage at the input of the pre-amplifier and the latched comparator. The pre-amplifier amplifies its own offset voltage, $V_{OA}=G_O V_{OSa}$, which is stored on the capacitors. This eliminates the contribution from V_{OSa} to the residual offset, because a zero difference at the pre-amplifier input yields a zero input voltage at the latched comparator. The residual offset is

$$V_{OS} = \left(1 + \frac{C_P}{C_S}\right)\left[\frac{\Delta q}{G_O C_S} + \frac{V_{OSl}}{G_o}\right] \qquad (3)$$

Equations (2) and (3) show that, for similar preamplifiers, the residual offset obtainable using OOS can be smaller than that for IOS.

IV. RESULT AND DISCUSSIONS

Performance analysis of preamplifier based dynamic comparator and its offset cancellations techniques are presented. Power dissipation (PD), propagation delay, offset voltage and number of transistors has been considered as performance metrics in the present analysis and investigations has been carried out at 130nm technology node [6]. All the circuits schematic are constructed on S-edit and results are obtained using TSPICE 13.0 version.
Fig. 4 shows the comparison of average power consumption between preamplifier based dynamic comparator and its offset optimization techniques i.e. output offset storage (OOS) technique and input offset storage (IOS) technique. For a good circuit, power consumption should be low as possible.

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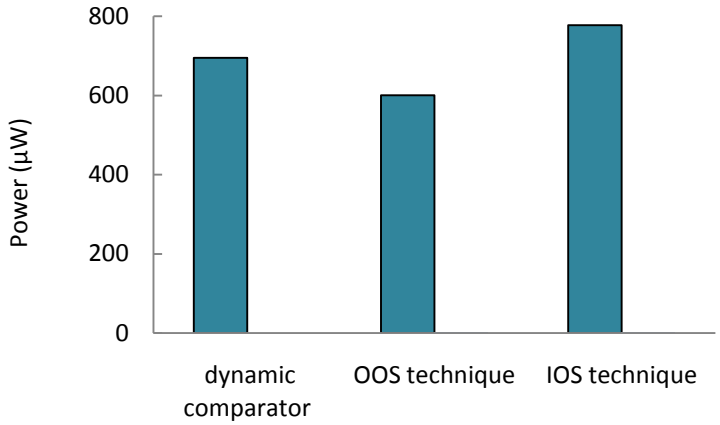

Fig. 4 Comparison of average power consumption between preamplifier based dynamic comparator and its offset voltage optimization techniques

Fig. 4 reveals that OOS technique has 13.57% and 22.76% less power consumption as compared to comparator before applying the offset reduction techniques and IOS technique respectively.
Preamplifier based dynamic comparator and its offset optimization techniques have been compared for propagation delay in Fig. 5. Delay of a circuit should be low as possible so that it can perform faster for a given signal. It has been concluded from the Fig. 5 that delay of comparator before applying the offset reduction techniques is 163.32% and 68.26% less than the OOS and IOS techniques respectively.

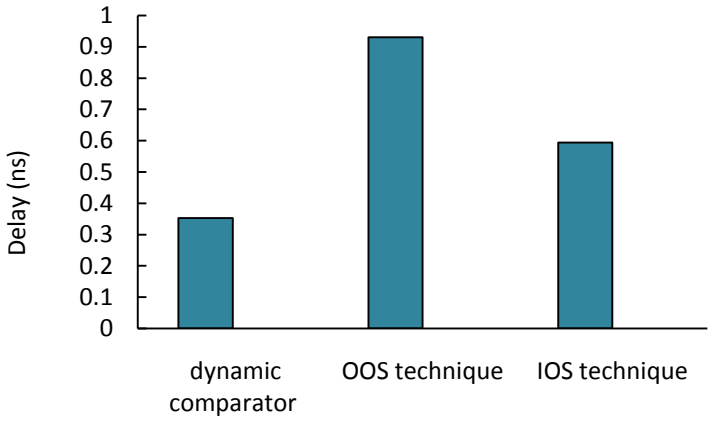

Fig. 5 Comparison of propagation delay between preamplifier based dynamic comparator and its offset voltage optimization techniques

Low power consumption can only be achieved at the expense of decreased operating speed (high delay) [7]. To trade-off between these two conflicting requirements it is useful to determine the power- delay product. Power-delay product is an important performance criterion as it depicts the energy consumption of the circuit. Lower the value of PDP the more effective is the circuit.

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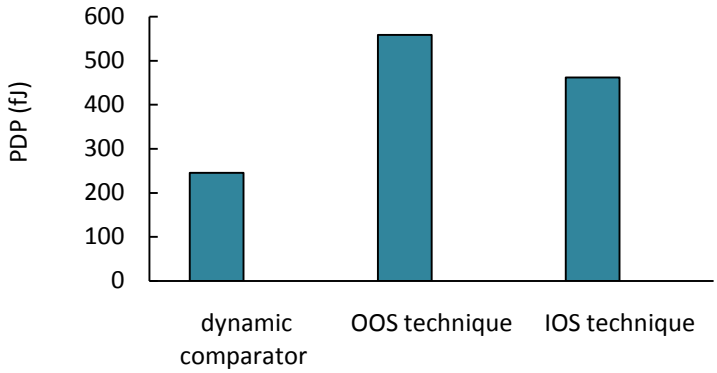

Fig. 6 Comparison of power-delay product between preamplifier based dynamic comparator and its offset voltage optimization techniques

Fig. 6 shows the comparison of power-delay product between preamplifier based dynamic comparator and its offset optimization techniques. Figure reveals that comparator before applying the offset reduction techniques consumes 56.06% and 46.89% less energy when compared to OOS and IOS offset reduction techniques respectively.

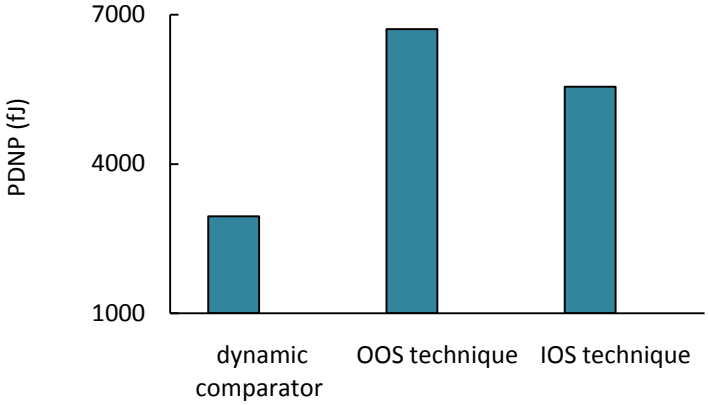

Fig. 7 Comparison of power-delay number product between preamplifier based dynamic comparator and its offset voltage optimization techniques

Power-delay and number of transistors product describes the silicon area requirement of a circuit. Fig. 7 shows the comparison of power-delay and number of transistors product between preamplifier based dynamic comparator and its offset optimization techniques. It can be concluded from the figure that OOS technique consumes 20.88% and 127.59% larger silicon area as compared to IOS technique and comparator before applying offset reduction technique respectively.

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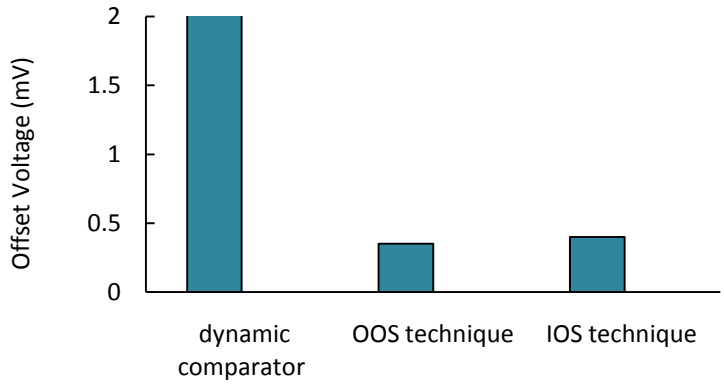

Fig. 8 Comparison of offset voltage between preamplifier based dynamic comparator and its offset voltage optimization techniques

Fig. 8 shows the comparison of offset voltage between preamplifier based dynamic comparator and its offset voltage optimization techniques. It is shown in the figure that a very large amount of offset voltage is reduced after applying offset reduction techniques i.e. 99.56% by IOS technique and 99.62% by OOS technique.
Output offset storage technique can be used to achieve higher accuracy as the amount of offset voltage reduced in output offset storage technique is 12.5% more than the input offset storage technique.

V. CONCLUSION

In this paper, preamplifier based dynamic CMOS comparator is optimized for offset voltage using charge storage techniques. Simulations have been performed to determine the minimum of offset voltage. Better results have been achieved after applying the optimization technique but at the same time both the reduction techniques has large power-delay product and power-delay number of transistor product. Thus high accuracy is only obtained at the expense of high energy consumption along with silicon area.

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BIOGRAPHY

Neerav Mehan received the Bachelor of Electronics and Communication Engineering degree from Institute of Engineering and Technology Baddi, Solan, H.P, India. She received the Master of Technology degree in VLSI from National Institute of Engineering Hamirpur, H.P, India. Since February 2011, she has been a Faculty with the Baddi University of Emerging Sciences and Technology, India. She is having around 03years of teaching and research experience. Her research interests include Analog VLSI and Digital VLSI.

Kamna Kohli received the Bachelor of Electronics and Communication Engineering degree from Institute of Engineering and Technology Baddi, Solan, H.P, India. She is pursuing Master of Technology degree in VLSI from B.B.S.B.E.C,

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Fatehgarh Sahib punjab, India. Since August 2007, she has been a Faculty with the Baddi University of Emerging Sciences and Technology, India. She is having around 06 years of teaching and research experience. Her research interests include image processing and Analog VLSI.

Anshul Kumar received the Bachelor of Electronics and Communication Engineering degree from International Institute of Telecom and Technology Kala Amb, Distt. Sirmour, H.P, India. He received the Master of Engineering degree in Digital Image Processing from Punjab Engineering College, Chandigarh India. Since July 2007, He has been a Faculty with the Engineering Institute of Emerging Sciences and Technology, now Baddi University India. He is having around 06 years of teaching and research experience. His research interests include Digital Signal Processing and Digital Image Processing, Analog VLSI.

Neha Sharma has been with Electronics & Communication Department of Baddi University of Emerging Sciences & Technology, Baddi. She has around 5 Years of teaching experience in courses like Wireless Communication, Microprocessors, and Optical fiber Communications & VLSI. Her current interest is high performance wireless networks & analog VLSI. She received her Bachelor of Technology degree from International Institute of Telecom and Technology, Nawanshahr, Punjab & Master of Technology degree in Communication Systems from Guru Nanak Dev University, Amritsar, Punjab, India.