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VLSI Implementation of Discrete Cosine Transform using modified CORDIC Algorithm

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ABSTRACT: In the latter years many of the architectures for discrete cosine transform (DCT) has been suggested and concluded that CORDIC (Coordinate-Rotation-Digital-Computer) processor based design is best suited and convenient for DCT design. CORDIC (Coordinate-Rotation-Digital-Computer) is division of shift and add phenomenon based principle for rotation of vector and rotation of plan, which is mainly used for the calculation of Trigonometric and Hyperbolic operations. CORDIC based architecture delivers iteration method and regulated like digit by digit operation. For these operation, it is pre-owned add, subtract, shifting of given bits and lookup table. Proposed architecture is compromise of input elements adding and subtracting, CORDIC module and output elements. Proposed Architecture is counterfeit for 8-point DCT and synthesized adopting Xilinx FPGA ISI 14.1i Vertex-5 device (xc5vfx100t-3ff1738) as a target device, which can engage at a maximum frequency of 184.556 MHZ.

KEYWORDS: - DCT, CORDIC, Shift and Add, Virtex-5, Number of Slice

I. INTRODUCTION

Advances in semiconductor technology are leading to a golden era for processing analog signals digitally. Digital signal processing (DSP) is the branch of engineering that performs a broad class of signal processing operations. We are surrounded by many devices that perform digital signal processing. The real-time DSP applications include: speech processing, spectral analysis, digital image processing, biomedical image processing, digital video compression, data compression, digital communication, and radar, to name a few [1]. The hardware implementation of any DSP application demands high-throughput and fewer resources for real-time operation. The discrete Cosine transform (DCT) performs a crucial role in digital signal processing and it is used for signal transformation and analyses. The critical operation involved in the computation of DCT is the complex twiddle multiplication. Novel modifications to the Co-ordinate Rotational Digital Computer (CORDIC) algorithm, are presented in this thesis to carry out the complex multiplication more efficiently with less hardware and latency [2, 3].

DCT based coding/decoding systems play a dominant role in real-time applications. However, the DCT is computationally intensive. In addition, 1-D DCT has been recommended by standard organizations the Joint Photographic Expert Group (JPEG) [1] .The standards developed by these groups aid industry manufacturers in developing real-time 1-D DCT chips for use in various image transmission and storage systems [4].

DCT based coding and decoding systems play a dominant role in real-time applications in science and engineering like audio and Images. VLSI DCT processor chips have become indispensable in real time coding systems because of their fast processing speed and high reliability. JPEG has defined an international standard for coding and compression of continuous tone- still images. This standard is commonly referred to as the JPEG standard [3]. The primary aim of the JPEG standard is to propose an image compression algorithm that would be generic, application independent and aid VLSI implementation of data compression. As the DCT core becomes a critical part in an image compression system, close studies on its performance and implementation are worthwhile and important. Application specific requirements are the basic concern in its design. In the last decade the advancement in data communication techniques was significant, during the explosive growth of the Internet the demand for using multimedia has increased [5].

Video and Audio data streams require a huge bandwidth to be transferred in an uncompressed form. Several ways of compressing multimedia streams evolved, some of them use the Discrete Cosine Transform (DCT) for transform coding and its inverse (IDCT) for transform decoding. Image compression is a useful topic in the digital world. A

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digital image bitmap can contain considerably large amounts of data causing exceptional overhead in both computational complexity as well as data processing. Storage media has exceptional capacity however access speeds are typically inversely proportional to capacity. Compression is a must to manage large amounts of data for network, internet, or storage media [5]. Compression techniques have been studied for years, and will continue to improve. Typically image and video compressors and decompressors (CODECS) are performed mainly in software as signal processors can manage these operations without incurring too much overhead in computation [6]. However, the complexity of these operations can be efficiently implemented in hardware. Hardware specific CODECS can be integrated into digital systems fairly easily. Improvements in speed occur primarily because the hardware is tailored to the compression algorithm rather than to handle a broad range of operations like a digital signal processor. Data compression itself is the process of reducing the amount of information into a smaller data set that can be used to represent, and reproduce the information [7]. Types of image compression include lossless compression, and lossy compression techniques that are used to meet the needs of specific applications.

II. DISCRETE COSINE TRANSFORM

Discrete Cosine Transformation (DCT) is the most widely used transformation algorithm. DCT, first proposed by way of Ahmed [9] et al, 1974, has got greater importance in current years, in particular in the fields of photograph Compression and Video Compression. This chapter makes a speciality of green hardware implementation of DCT by way of reducing the variety of computations, enhancing the accuracy of reconstruction of the unique information, and lowering chip place. due to which the electricity consumption additionally decreases. DCT also improves velocity, compared to different trendy picture compression algorithms like JPEG.

DCT output

$$F(0) = 0.5(f(0) + f(1) + f(2) + f(3) + f(4) + f(5) + f(6) + f(7))\cos\frac{\pi}{4}$$

$$F(1) = 0.5[\{(f(0) - f(7)\}\cos\frac{\pi}{16} + \{f(1) - f(6)\}\cos\frac{3\pi}{16} + \{f(2) - f(5)\}\cos\frac{5\pi}{16} + \{f(3) + f(4)\}\cos\frac{7\pi}{16}]$$

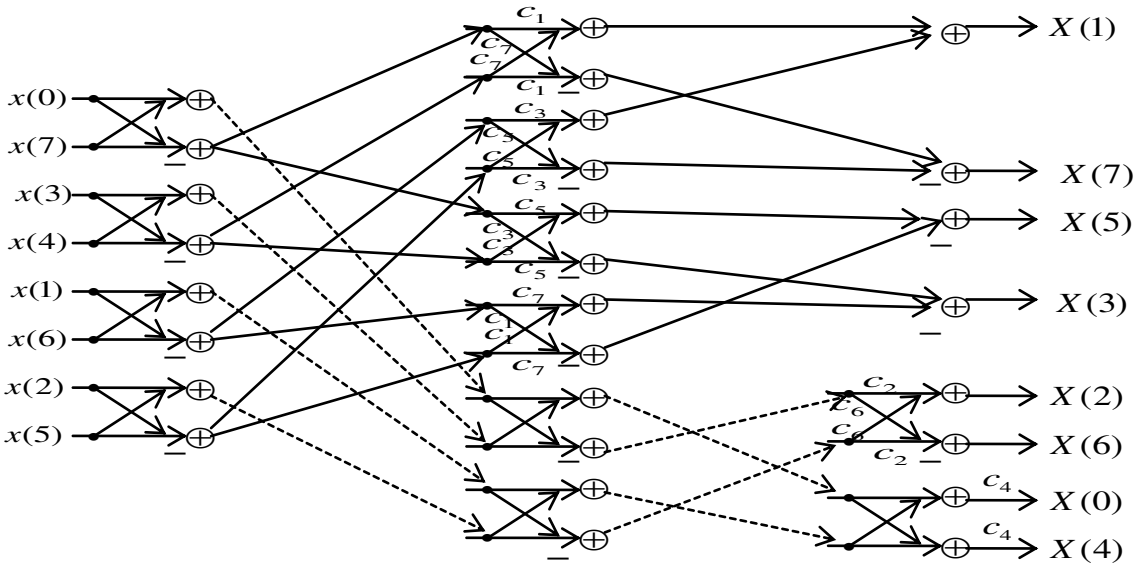

Figure 1: 8-point Discrete Cosine Transform

$$F(2) = 0.5[\{(f(0) - f(3) - f(4) + f(7)\}\cos\frac{2\pi}{16} + \{f(1) - f(2) - f(5) + f(6)\}\cos\frac{6\pi}{16}]$$

$$F(3) = 0.5[\{(f(0) - f(7)\}\cos\frac{3\pi}{16} + \{f(6) - f(1)\}\cos\frac{7\pi}{16} + \{f(5) - f(2)\}\cos\frac{\pi}{16} + \{f(4) + f(3)\}\cos\frac{5\pi}{16}]$$

$$F(4) = 0.5[(f(0) + f(3) + f(4) + f(7) - f(1) - f(2) - f(5) - f(6))\cos\frac{\pi}{4}]$$

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$$F(5) = 0.5[\{(f(0) - f(7)\}\cos\frac{5\pi}{16} + \{f(6) - f(1)\}\cos\frac{\pi}{16} + \{f(2) - f(5)\}\cos\frac{7\pi}{16} + \{f(3) + f(4)\}\cos\frac{3\pi}{16}]$$

$$F(6) = 0.5[\{(f(0) - f(3) - f(4) + f(7)\}\cos\frac{6\pi}{16} - \{f(1) - f(2) - f(5) + f(6)\}\cos\frac{2\pi}{16}]$$

$$F(7) = 0.5[\{(f(0) - f(7)\}\cos\frac{7\pi}{16} + \{f(6) - f(1)\}\cos\frac{5\pi}{16} + \{f(2) - f(5)\}\cos\frac{3\pi}{16} + \{f(4) + f(3)\}\cos\frac{\pi}{16}]$$

III. CORDIC ALGORITHM

The simple form of CORDIC is based on observation that if a unit length vector with an (x,y)=(1,0) is rotated by an angle αdegrees, its new end point will be at $(x, y) = (\sin\alpha, \cos\alpha)$ thus coordinates can be computed by finding the coordinates of new end point of the vector after rotation by an angle α. Rotation of any (x, y) vector:

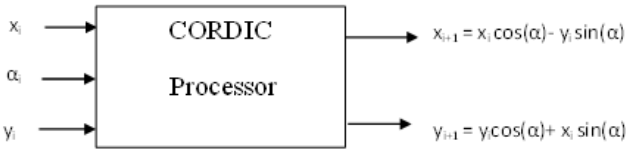

Figure 2: Block Diagram of CORDIC Processor

Basic equation of CORDIC algorithm

$$x_{i+1} = x_i\cos(\alpha) - y_i\sin(\alpha) \quad (1)$$

$$y_{i+1} = y_i\cos(\alpha) + x_i\sin(\alpha) \quad (2)$$

Rearrange equations

$$x_{i+1} = \cos(\alpha)[x - y\tan\alpha] \quad (3)$$

$$y_{i+1} = \cos(\alpha)[y + x\tan\alpha] \quad (4)$$

$$\tan\alpha = \frac{\sin\alpha}{\cos\alpha}$$

IV. PROPOSED METHODOLOGY

This algorithm performs its computation by decomposing the transform of size 'N' into 2 equal transforms of size N/r at each phase for a computation. When all such small elements are combined together conducive to compute DCT then it is known as DCT butterfly unit of '2' size. The flow graph of the proposed DCT architecture is displayed in Figure 3.

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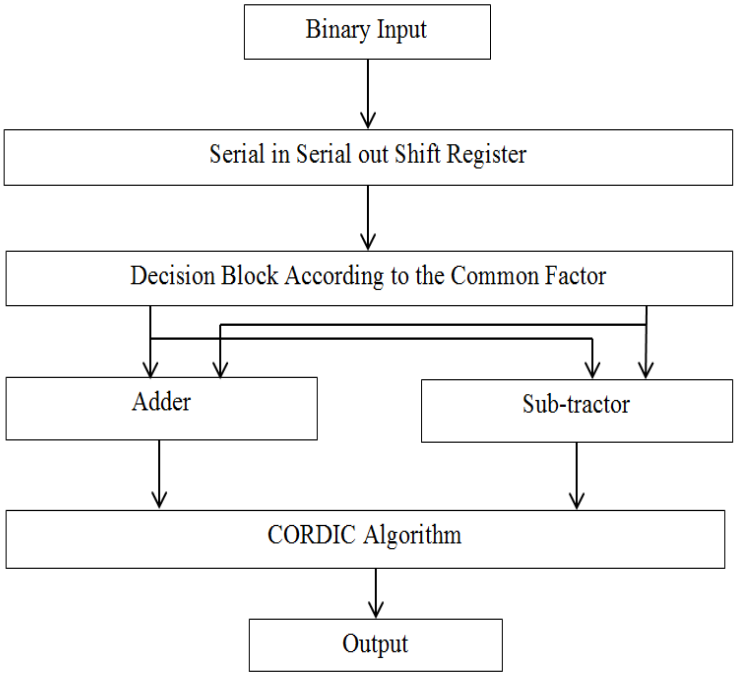

Figure 3: Flow Chart of the Proposed DCT Architecture

Step-I: - The binary input function is a signal conditioning device that interfaces to the serial-in-serial-out shift register. All integer number applied to the binary form in DCT architecture. Binary input is leaning on the word limit i.e. suppose word limit of the binary input (3 down to 0) means the input range is 0 to 15.
Step-II: - Second block of the proposed DCT architecture is serial-in-serial-out shift register. With the support of flips-flops, Serial-in-serial-out shift register can be developed. The register is firstly cleaned, suppress all output of the serial-in-serial-out shift register becomes to zero. The initial-sequentially-tuned input data is then feed to the as an input signal of the first flip-flop of the left. During each and every clock pulse, one bit is broadcast from left to right.
Step-III: - Third block of the proposed DCT architecture is decision block. According to the number the block is select and gives the output of the adder and sub-tractor. There are condition is applied of the decision block based on common term of the DCT output equation.
Step-IV: - Conferring to the decision multiplier block it used adder and sub-tractor block.
Step-V: - And last of the algorithm are used to CORDIC algorithm. CORDIC algorithm handles two inputs per clock and so two output samples are processed per clock cycle. The advantage of the CORDIC technique is minimized delay overall system.
Figure 4 shows the DCT using a CORDIC architecture is explain, in which clearly observed there are eight input from f(0) to f(8). All the input are pairing i.e. f(0) to f(7), f(2) to f(5), f(4) to f(3) and f(1) to f(6), because the common are term are used in all the pair. In these architecture seven adders, nine sub-tractors and six CORDIC architectures are used. CORDIC architecture is depends on rotation, shifter and addition. CORDIC algorithm is recognizable selection line.

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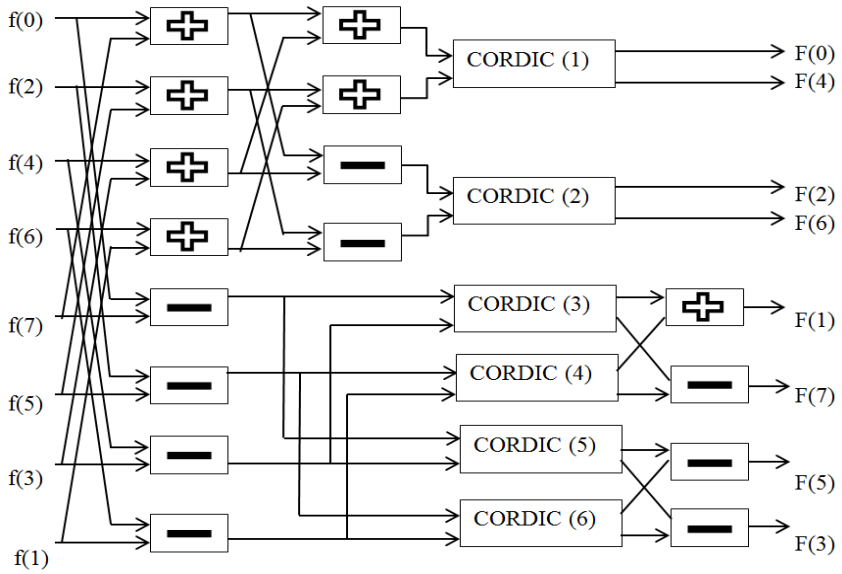

Figure 4: Architecture for DCT using CORDIC

Table 1 shows how i is selected during each iterations of the equation. If the rotations positive, the rotation of unit vector takes place in a negative direction, the X variable is reduced by a fraction of the Y variable, and Y variable is incremented by a fraction of the X variable. If the angle is negative, the opposite operation is performance for each variable.

Table 1: Rotation Parameter for CORDIC Algorithm

CORDIC Iteration d, i				
Processor	CORDIC(1)	CORDIC(2)	CORDIC(3)(6)	CORDIC(4)(5)
	$\frac{\pi}{4}$	$\frac{3\pi}{8}$	$\frac{7\pi}{16}$	$\frac{3\pi}{16}$
1	+1,0	+1,0	+1,0	+1,1
2		+1,2	+1,1	+1,3
3		+1,3	+1,3	+1,10
4		+1,6	+1,10	
5		+1,7		
6		+1,9		

V. SIMULATION RESULT

Given experiment shows that there are 16-bit, 8 inputs f0, f1, f2, f3, f4, f5, f6, and f7 are simulated throw Xilinx 14.1i VHDL test bench simulation for DCT calculation and result was obtained. Final output displayed in table 5.1 as k1, k2, k3, k4, k5, k6, k7, k8.

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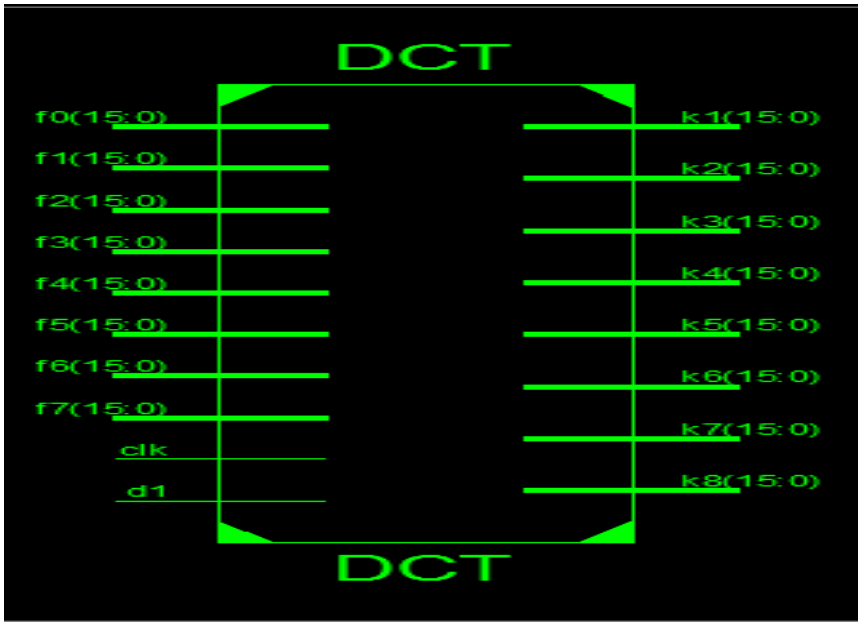

Figure 5: Resister transfer Level (RTL) View of 8-point

The proposed DCT implementation using CORDIC algorithm gives a lower slice 342 as compared with 1102 for previous DCT implementation using multiplier based algorithm. The proposed method is 31.03% improved in previous algorithm in the field of number of slice register. The proposed DCT implementation using CORDIC algorithm gives lower LUTs 1303 as compared with 2551 for previous DCT implementation using multiplier based algorithm. The proposed method is 51.28% improved in previous algorithm in the field of number of LUTs. The proposed DCT implementation using CORDIC algorithm gives a lowers maximum frequency 184.556 MHz as compared with 224.9 MHz for previous DCT implementation using multiplier based algorithm. The proposed method is 17.09% improved in previous algorithm in the field of number of Maximum Frequency. The proposed DCT implementation using CORDIC algorithm gives a lower No. of IOBs 238 as compared with 1588 for previous DCT implementation using multiplier based algorithm. The proposed method is 74.35% improved in previous algorithm in the field of No. of IOBs. The Bar Graph for the DCT Different Architecture according to the percentage win is given next.

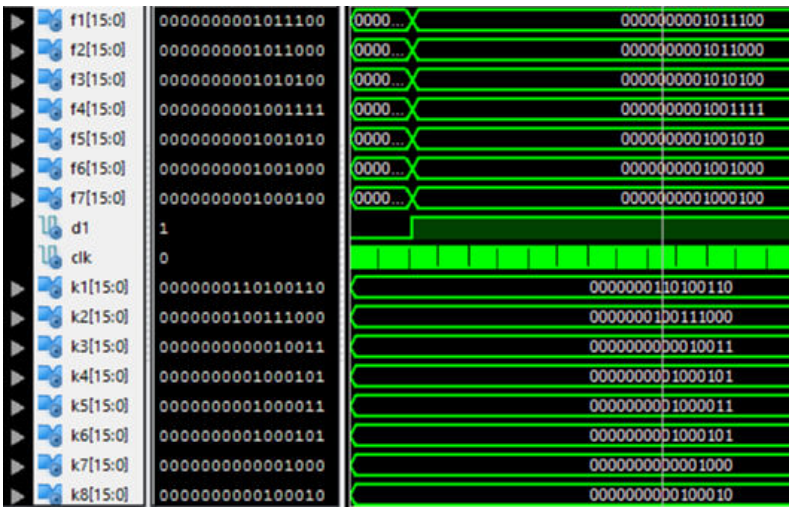

Figure 6: Output Waveform of Proposed 8-point DCT

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Table 2: Device Utilization for DCT Algorithm

	Previous Algorithm	Proposed Algorithm
Adder	47	34
Multiplier	2	0
Number of Register	742	342
Logic Cell	1544	1303
LUT-FF Pairs	412	236
Memory	552960 Kbit	482845 Kbit
Maximum Frequency Operation	105.4 MHz	184.556 z

VI. CONCLUSION

In many real-time applications, high-performance is required by DSP systems. The DCT performs a crucial role in the field of DSP as DCT is used in many DSP applications for signal transformation and analyses. High-performance with fewer hardware resources is highly desirable for any real-time application. Need for a complex multiplier to carry out the multiplication of complex twiddle factors and large memory to store the twiddle factors are the main concerns for FFT implementation. In this thesis, the well-known CORDIC algorithms and their architectures are studied. The significance of the CORDIC algorithm in real-time DSP applications is presented. The implemented DCT designs using CORDIC algorithm are consume less percentage of given parameters, which are 30.03% of slice register, 48.72% of logic cell, 51.28 % of fully used LUT-FF pairs, 74.35% of memory and 17.9% maximum frequency compared to previous algorithm. This is greatly reducing the area as compared to previous algorithm.

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