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# Parallel-Prefix Adders Implementation Using Reverse Converter Design

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**ABSTRACT:** In this brief, the design of reverse converter using parallel prefix adder based multiplier for residue number system is proposed. Nowadays the parallel prefix adders are not used even though it provides significant delay reduction and high speed operation because of higher power consumption. The novel specific hybrid parallel prefix adder components that compensate the delay and power consumption in the existing system is applied to design the reverse converter. Different parallel adder structures are analyzed among that the Brent Kung prefix network is used for the parallel prefix addition because of the minimum fan-out. In the proposed system the high speed parallel prefix adder is designed for modulo(4n+1) addition for n=5 and thereby designing the multiplier by using the shifting operation in the same design.

**KEYWORDS:** Digital arithmetic, parallel-prefix adder, residue number system (RNS), reverse converter

## I. INTRODUCTION

IN THE world of battery-based and portable devices, the residue number system (RNS) can play a significant role due to its low power features and competitive delay. The RNS can provide carry free and fully parallel arithmetic operations for several applications, including digital signal processing and cryptography. However, its real usage requires forward and reverse converters to be integrated in the existing digital systems. The reverse conversion, i.e., residue to binary conversion, is a hard and time-consuming operation. Hence, the problem of designing high-performance reverse converters has motivated continuous research using two main approaches to improve the performance of the converters: 1) investigate new algorithms and novel arithmetic formulations to achieve simplified conversion formulas and 2) introduce new moduli sets, which can lead to more simple formulations. Thereafter, given the final simplified conversion equations, they are computed using well-known adder architectures, such as carry-save adders (CSAs) and ripple-carry architectures, to implement carry-propagate adders (CPAs) and, more seldomly, fast and expensive adders such as the ones with carry-look ahead or parallel-prefix architectures.

In this brief, for the first time, we present a comprehensive methodology to wisely employ parallel-prefix adders in carefully selected positions in order to design fast reverse converters. The collected experimental results based on area, delay, and power consumption show that, as expected, the usage of the parallel-prefix adders to implement converters highly increases the speed at the expense of additional area and remarkable increase of power consumption. The significant growing of power consumption makes the reverse converter not competitive. Two power-efficient and low-area hybrid parallel-prefix adders are presented in this brief to tackle with these performance limitations, leading to significant reduction of the power delay product (PDP) metric and considerable improvements in the area-time2 product (AT2) in comparison with the original converters without using parallel-prefix adders.

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## II. BACKGROUND

The forward converter, modulo arithmetic units, and reverse converter are the main parts of the RNS. In contrast to other parts, reverse converter consists of a complex and non-modular structure. Therefore, more attention should be directed to its design to prevent slow operation and

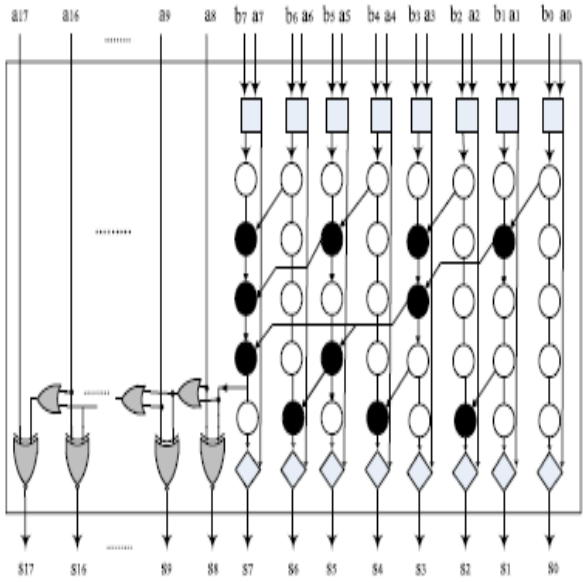

Fig. 1. HRPX structure with BK prefix network.

compromise the benefits of the RNS. Both the characteristics of the moduli set and conversion algorithm have significant effects on the reverse converter performance. Hence, distinct moduli sets have been introduced. In addition to the moduli set, hardware components selection is key to the RNS performance. For instance, parallel-prefix adders are known as unsuitable structures for complex reverse converters because of their high power consumption. However, parallel-prefix adders with its high-speed feature have been used in the RNS modular arithmetic channels. This performance gain is due to parallel carry computation structures, which is based on different algorithms. Each of these structures has distinct characteristics, such as Sklansky (SK), and Kogge–Stone (KS) have the maximum and minimum fan-out, respectively, both providing minimal logic depth. Minimum fan-out comes at the expense of more circuit area. Therefore, hardware components selection should be undertaken carefully.

## III. NEW PARALLEL-PREFIX-BASED COMPONENTS

The Chinese remainder theorem, or other related improved
approaches and techniques underlie the RNS reverse conversion, whose formulation can be directly mapped to ripple-carry adders (RCA). However, this leads to significant speed degradation, due to the linear increase of the delay in the RCA with the number of bits. Parallel-prefix adders can be used in the RNS reverse converters to bind the delay to logarithmic growth. However, in reverse converters, several parallel-prefix adders are usually required. Even when only one adder is used, the bit length of this adder is quite large. Consequently, this results in high power consumption notwithstanding its high speed.

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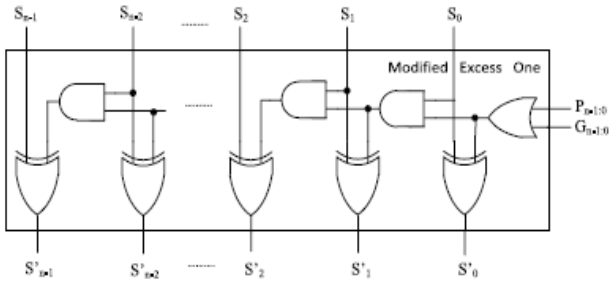


Fig. 2. Modified excess-one unit.

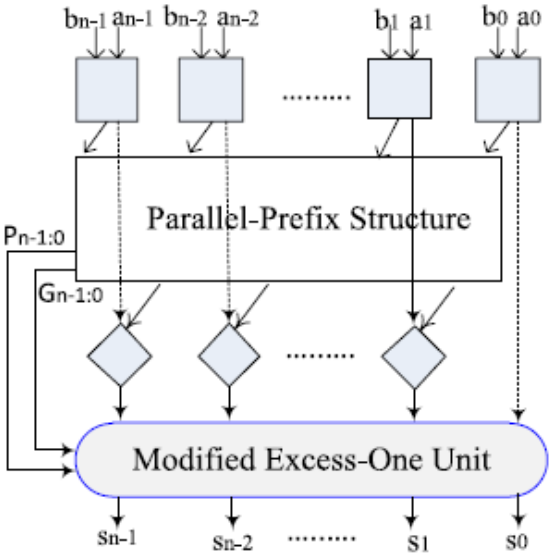


Fig. 3. HMPE structure.

Therefore, in this section, two approaches that take advantage of the delay properties of the parallel prefix adders with competitive power consumption are introduced. Usually, one regular binary addition is required in reverse converter structures to achieve the final binary representation. This final addition has an important effect in the total delay of the converter due to the large bit-length of the operands. the modulo $2n - 1$ addition is an essential operation in the reverse conversion for most moduli sets. The regular CPA with end around carry (EAC) is by default a moduli $2n - 1$ adder with double representation of zero, but in reverse converters a single representation of zero is required. So, a one detector circuit has to be used to correct the result, which imposes an additional delay. However, there is a binary-to-excess-one converter (BEC), which can be modified to fix the double-representation of zero issue.

The main reason for the high power consumption and area overhead of these adders is the recursive effect of generating and propagating signals at each prefix level. An optimized approach is proposed, which uses an extra prefix level to add the output carry. However, this method suffers from high fan-out, which can make it usable only for small width operands. However, we could address this problem by

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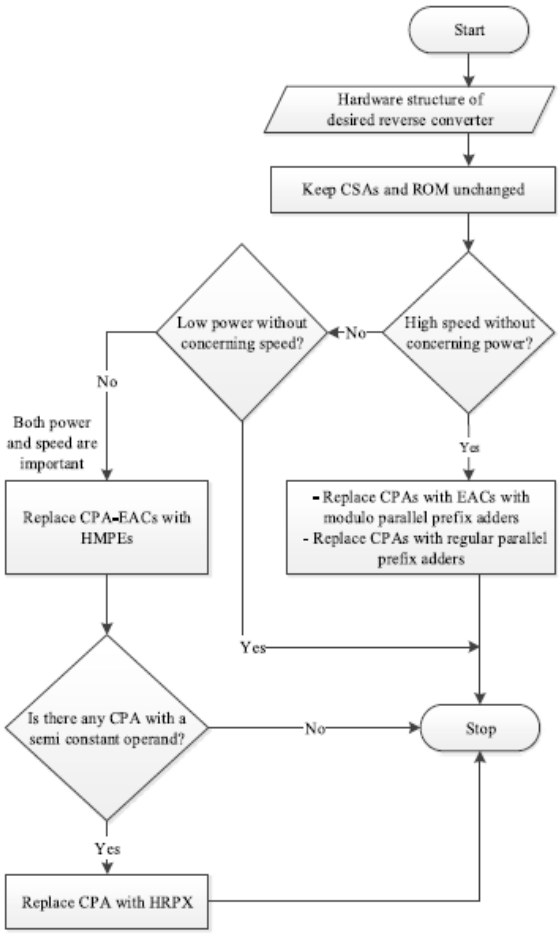


Fig. 4. Reverse converter design methodology.

eliminating the additional prefix level and using a modified excess-one unit instead. In contrast to the BEC, this modified unit is able to perform a conditional increment based on control signals as shown in Fig. 2, and the resulted hybrid modular parallel-prefix excess-one (HMPE) adder is depicted in Fig. 3. The HMPE consists of two parts: 1) a regular prefix adder and 2) a modified excess one unit. First, two operands are added using the prefix adder, and the result is conditionally incremented afterward based on control signals generated by the prefix section so as to assure the single zero representation.

Summarizing, the HMPE is highly flexible, since it can be used with every prefix networks. Hence, the circuit performance metrics such as area, delay, and power-consumption can be adjusted by selecting the desired prefix structure. On the other hand, the HRPX avoids the usage of a large size parallel-prefix adder with high power consumption, and also does not have the penalty of using the long carry-propagation chain of a RCA

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## IV. REVERSE CONVERTER DESIGN METHODOLOGY

In this section, the methodology of reverse converter design is described. In the following, a method employing distinct components in the architecture of the reverse converter will be presented. Several reverse converters for different moduli sets have been introduced, which can be classified into three classes. The first class consists of converters with a tree of CSAs with EAC followed by a two-operand modulo $2k - 1$ CPA. A second class includes more complex reverse converters, which have several CSAs and CPAs with EACs followed by a final regular subtractor with two operands of different size. The implementation of this subtractor using regular binary-adder results in one operand with some constant bits. The third class covers the reverse converters that have been designed for moduli sets with moduli other than the popular $2n$ and $2n \pm 1$.

In the following, we describe a methodology for designing reverse converters in the first and second classes. The suggested method for applying the HMPE and HRPX in the reverse converter is shown in Fig. 4.

First of all, it is relevant to decide about the required performance metrics based on the specified application. If it is just important to achieve the least power consumption and hardware cost without considering speed, no prefix adder is needed. On the other hand, if high speed is the designer goal, the CPAs with EAC and the regular CPAs should be replaced by traditional parallel prefix modulo $2n - 1$ adders and regular parallel-prefix adders, respectively. However, for the VLSI designers, a suitable tradeoff between speed, power, and area is often more important. In this case, first, CPAs with the EAC can be replaced by the HMPEs. Then, if the converter contains a regular CPA where one of its operands has a string of constant bits with the value of one, it can be replaced with the HRPX.

## V. VLSI IMPLEMENTATIONS

In order to support a thorough assessment, especially for power consumption, the proposed method was applied to three different reverse converters and application-specific integrated circuits (ASICs) were implemented. The target reverse converters are: 1) the Converter-1 for moduli set $\{2n - 1, 2n, 2n+1, 22n+1- 1\}$;2) the Converter-2 for $\{2n - 1, 2n+1, 22n, 22n+1 - 1\}$; and3) the Converter-3 for $\{2n - 1, 2n+1, 22n, 22n+1\}$. The architectures of these converters are proposed, each of them is configured based on the Fig. 4 methodology. The implemented converters can be classified as follows: 1) cost effective designs using only the RCAs for the CPAs with the EAC and regular CPAs; 2) speed efficient designs, which substitute all the CPAs with EAC and the regular CPA by the parallel-prefix modulo $2n - 1$ adders of Type-I, and KS regular parallel-prefix adders, respectively; and 3) designs that use both HMPE and HRPX, tradeoff between circuit parameters. Three well-known approaches for prefix network, i.e., Brent–Kung

TABLE-**I**

COMPARING POWER, $AT^2$, AND PDP FOR MODULI $\{2^n - 1, 2^n+1, 2^{2n}, 2^{2n}+1\}$ CONVERTERS

| Converter 3 | Power (mW) | | | | $AT^2$ | | | | PDP | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Structure | 4 | 8 | 12 | 16 | 4 | 8 | 12 | 16 | 4 | 8 | 12 | 16 |
| RCA-based Adders | 4.446 | 5.42 | 6.382 | 6.997 | 397.98 | 1493.61 | 3393.72 | 6396.03 | 2.22 | 3.97 | 5.81 | 7.65 |
| Fully Prefix Adders | 15.04 | 25.5 | 39.99 | 53.85 | 107.72 | 333.37 | 509.02 | 835.61 | 3.34 | 6.83 | 10.72 | 15.72 |
| **HMPE-KS** | 17.47 | 28.11 | 37.56 | 26.52 | 91.31 | 326.93 | 600.81 | 1755.74 | 3.55 | 7.53 | 11.04 | 11.72 |
| **HMPE-SK** | 11.47 | 21.02 | 16.75 | 19.87 | 95.12 | 231.34 | 848.65 | 1356.78 | 2.66 | 5.47 | 6.97 | 9.06 |
| **HMPE-BK** | 11.77 | 21.11 | 27.59 | 20.48 | 107.14 | 265.77 | 407.65 | 1341.29 | 2.85 | 5.70 | 7.86 | 9.32 |

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(BK), SK, and KS, have been considered for implementing the required prefix network in the proposed designs.

Finally, the practical interest of the proposed approaches can be verified in Tables. Our main goal is to decrease the cost of achieving high speed converters using parallel-prefix adders and also to provide applicable competitive tradeoff between power consumption and delay. For instance, with the HMPE and HRPX-SK converter for $n$ = 16%, 63% of the power is saved at the expense of 35% delay increase, and also 42% of improvement in the PDP is achieved when compared with fully parallel-prefix adders based designs. In the other hand, the proposed designs consume more power to achieve higher speed than the RCA-based ones.

## VI. SIMULATION RESULTS

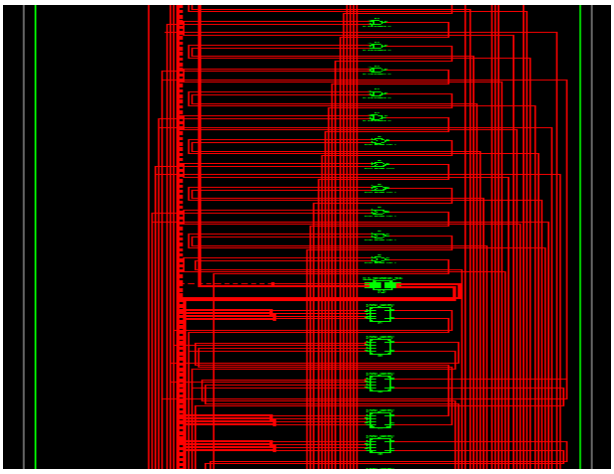

Fig: RTL Schematic of HRPX-BK

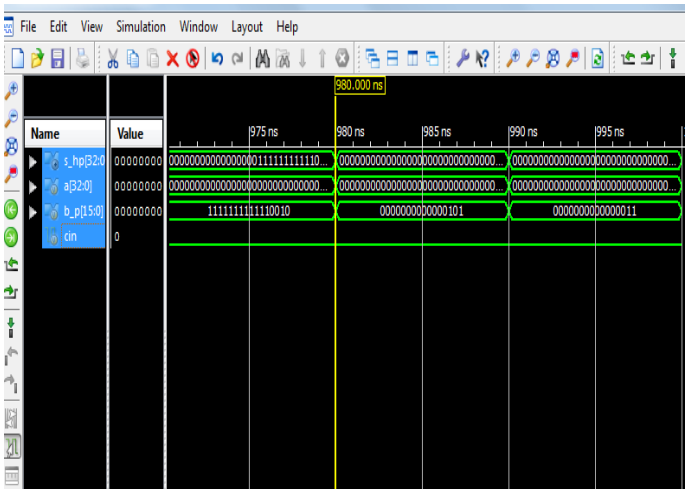


Fig: WAVEFORMS OF HRPX-BK

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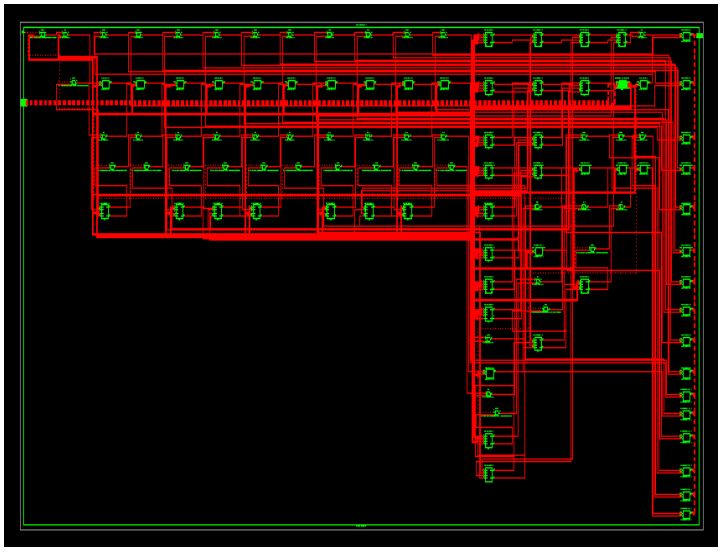

Fig: RTL SCHEMATIC OF HMPE-BK

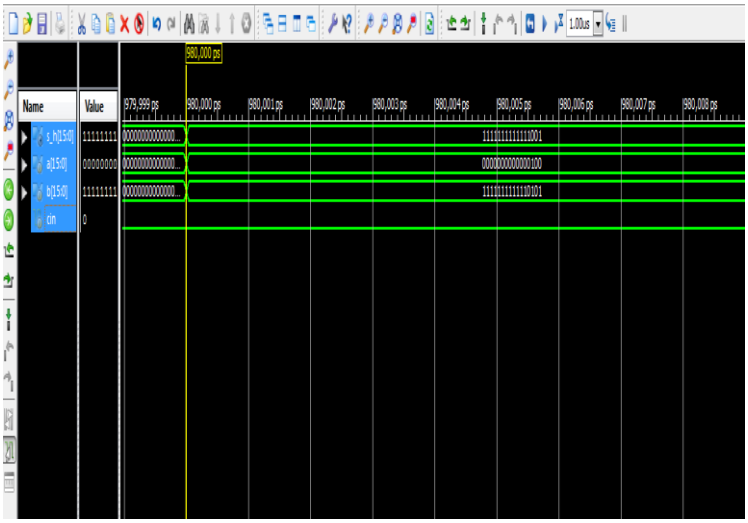


Fig: WAVEFORMS OF HMPE-BK

## V. CONCLUSION

This brief presents a method that can be applied to most of the current reverse converter architectures to enhance their performance and adjust the cost/performance to the application specifications. Furthermore, in order to provide the required tradeoffs between performance and cost, new parallel-prefix-based adder components were introduced. These components are specially designed for reverse converters. Implementation results show that the reverse converters based on the suggested

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components considerably improve the speed when compared with the original converters, which do not use any parallel-prefix adder, and reduce the power consumption compared with the converters that exclusively adopt parallel-prefix adders.

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