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Realization of Soft Processor Using Xilinx

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ABSTRACT: This project presents the design of 8-bit processor by using verilog HDL in Xilinx ISE12.2 simulator. The 8-bit processor consists of 8-bit ALU, 8-bit instruction register, 8-bit accumulator, 10-bit program counter, control unit and 8-bit temporary registers, which are 'a' register, 'b' register and 'y' register. It performs 22 different arithmetic and logical instructions such as addition, subtraction, increment, decrement, multiplication, square, ex-or, ex-nor, and, nand, nor, or, not, arithmetic shift left, arithmetic shift right, rotate left, rotate right, compare, logical shift left, logical shift right, add with carry, and subtract with carry. The control unit generates all the control signals needed for the coordination among the entire components of the processor. All the modules in the design were coded by using structural and behavioral modeling in verilog HDL language. The design entry, synthesis, and simulation of processor have been done by using Xilinx ISE 12.2 software. The processor is designed with 5% utilization and totally 328 slices are used. Its frequency is 1MHz which is obtained, with a minimum period of 1000ns.

KEYWORDS: 8-bit processor, verilog HDL, Xilinx ISE12.2, Arithmetic and logic unit (ALU).

I. INTRODUCTION

The achievements in the area of microelectronics have brought a revolution in the field of computers. The advent of integrated circuit in 1957 was the turning point. It was possible by 1990 to put more than 80,000 transistors on a single chip using NMOS technology. Simultaneously, CMOS offers low power requirement, which is vital for many applications. Due to these advancements in microelectronics technology, it became possible to put ALU and Control Unit on a single IC chip. This integrated circuit is called microprocessor. The processor or Central Processing Unit (CPU) is the heart of the computer. A microprocessor is a single integrated circuit that contains all the functionality of a central processing unit (CPU), processes computer instructions. CPU determines how fast the computer will be and what capabilities the machine will have. The microprocessor is considered a major revolution in the field of computers. It has also been made possible to integrate ALU, Control unit and Memory on a single IC chip. This IC chip is called microcomputer. The microelectronics technology is continually advancing and consequently the microprocessors are becoming more powerful. Nowadays, microprocessors are used in a variety of electronic products such as cell phones, computer and robots etc,. It consists of thousands of electronic components and uses a collection of machine instructions to perform mathematical operations as well as to move information from one memory location to another.

II. RELATED WORK

Several papers regarding 8-bit processor has been reviewed. The following papers have been surveyed. In [1] Qasem Abu Al-Haija, Hasan Al-Amri, Mohamed Al-Nashri and Sultan Al-Muhaisen designed 4-bit microprocessor. In this paper 4-bit microprocessor with an instruction set architecture and microcode programming has been designed using the hardware modules and the software simulator. This microprocessor consists of Arithmetic and Logic Unit(ALU) and six registers. The six registers are 4-bit accumulator, flag register that holds zero and carry flags, Program counter(PC), Instruction register(IR), Memory address register(MAR), and Memory buffer register(MBR). All programs and data are stored in memory. Arithmetic and logic unit performs 8 arithmetic and logical operations. In [2] Paul Metzgen designed 32-bit ALU which presents the design of the arithmetic and logic unit used in Altera's NIOS 2.0 soft processor implemented on Altera's Apex 20KE FPGA architecture. This arithmetic and logic unit enabled the 32-bit NIOS 2.0 to consume only 1200 LEs and run at 85MHz. This is a 50% size reduction and 70% speed improvement over its predecessor, NIOS 1.1. In [4] Shridhar Devamane, Akshada Hanchate, Usha Vagare, Shalaka Ujagare, Pushpa Teggelli designed and implemented FPGA based Barrel shifter. It can be implemented as a sequence

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of multiplexer in which the output of one multiplexer is connected to the input of the next cascaded multiplexer in a way that depends on the shift distance. Barrel shifters are used to shift a desired number of bits in a desired direction in arithmetic and logic operations.

III. 8-BIT ALU DESIGN

ALU has been designed using verilog HDL. The Figure.1 shows a block diagram of ALU. Arithmetic unit and logic unit inputs 'a' and 'b' are fetched from registers. The output of arithmetic unit and logic unit are given to 32:1 multiplexer. A 32:1 multiplexer requires 5 selection lines which are s0, s1, s2, s3, s4. According to this selection lines arithmetic and logical operations will perform. Finally ALU output stored in 'y' register. After the execution of any arithmetic and logical instruction, if the result is zero, the zero flag is set. The sign flag is set, when bit D7 of the result is 1. This flag is used with signed numbers. In a given byte, if D7 is 1, the numbers will be positive number; otherwise it will be negative number. The zero flag is set if ALU operation results in 0.

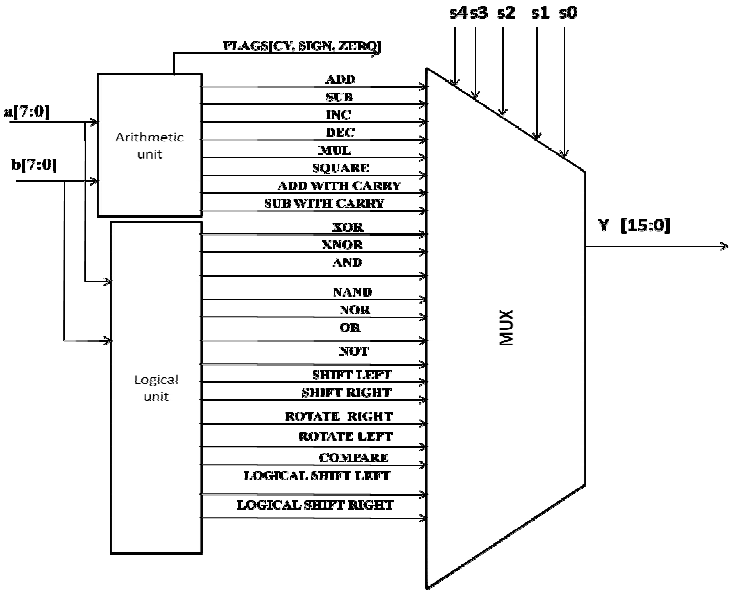

Figure.1 Block diagram of 8-bit ALU

A. ALU operations

ALU performs 22 different arithmetic and logical operations, which are given in the Table. 1. All the ALU operations in the design were coded by using structural and behavioral modeling in verilog HDL language.

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Table.1

Selection line	Function	Operation
00000	Addition	Y←a+b
00001	Subtraction	Y←a-b
00010	Increment	Y←a+1
00011	Decrement	Y←a-1
00100	Multiplication	Y←a*b
00101	Square	Y←a*a
00110	Ex-or	Y←a^b
00111	Ex-nor	Y←~(a^b)
01000	AND	Y←a&b
01001	NAND	Y←~(a&b)
01010	NOR	Y←~(a|b)
01011	OR	Y←a|b
01100	NOT	Y←~a
01101	Arithmetic shift left	Y←Arithmetic shift left 'a'
01110	Arithmetic shift right	Y←Arithmetic shift right 'a'
01111	Rotate left	Y←Rotate left'a'
10000	Rotate right	Y←Rotate right 'a'
10001	Compare	Y←Compare'a' and 'b'
10010	Logical shift left	Y←Logical shift left 'a'
10011	Logical shift right	Y←Logical shift right 'a'
10100	Add with carry	Y←a+b+1
10101	Subtract with carry	Y←a-b+1

IV. MEMORY

Memory stores the bulk of data, instructions and results. The basic unit of memory is called word. A word can store one unit of data. Each memory location is associated with an address, which is used to access that particular location. With every read or write operation on the memory, the address where the operation is to be performed is also specified. Memory address range of 1K (1024×8) memory shown in Figure.2. The memory chip has 1024 registers; therefore 10 address lines (A9 –A0) are required to identify the registers. Each register hold 8-bit data. The memory chip is enabled when the chip select signal is 1.The address lines A9-A0 can assume any address of the 1024 registers, starting from all 0s to all 1s, as shown below

A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
0 0 0 0 0 0 0 0 0 0 =000H
A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
1 1 1 1 1 1 1 1 1 1 =3FFH
The memory addresses range from 000H to 3FFH.

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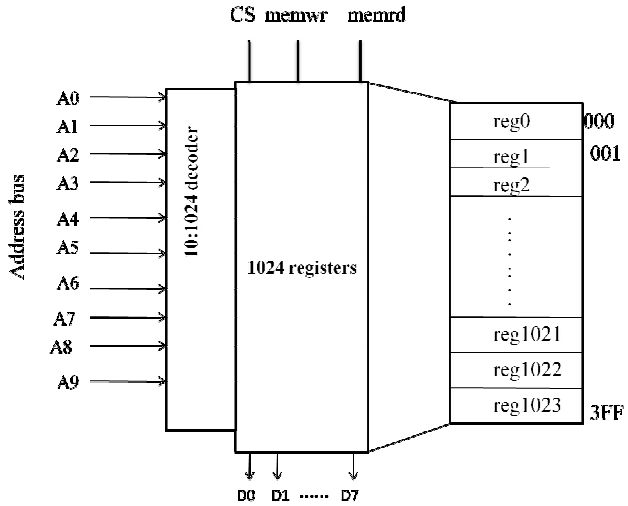

Figure.2 Block diagram of memory

V. PROPOSED PROCESSOR ARCHITECTURE

The proposed system architecture is shown in Figure. 3. It executes 22 different arithmetic and logical instructions such as addition, subtraction, increment, decrement, multiplication, square, ex-or, ex-nor, and, nand, nor, or, not, arithmetic shift left, arithmetic shift right, rotate left, rotate right, compare, logical shift left, logical shift right, add with carry, and subtract with carry.

To fetch the instruction in memory location 1008H, the following steps are performed:

1. The program counter places the 10-bit address 1008H of the memory location on the address bus.
2. The control unit send the memory read control signal (memrd=1) to enable read operation.
3. After receiving read signal from memory, the instruction (01H) stored in the memory location is placed on the data bus and transferred to instruction register (IR).
4. The instruction present in the IR is decoded and executed according to the binary pattern of the instruction.

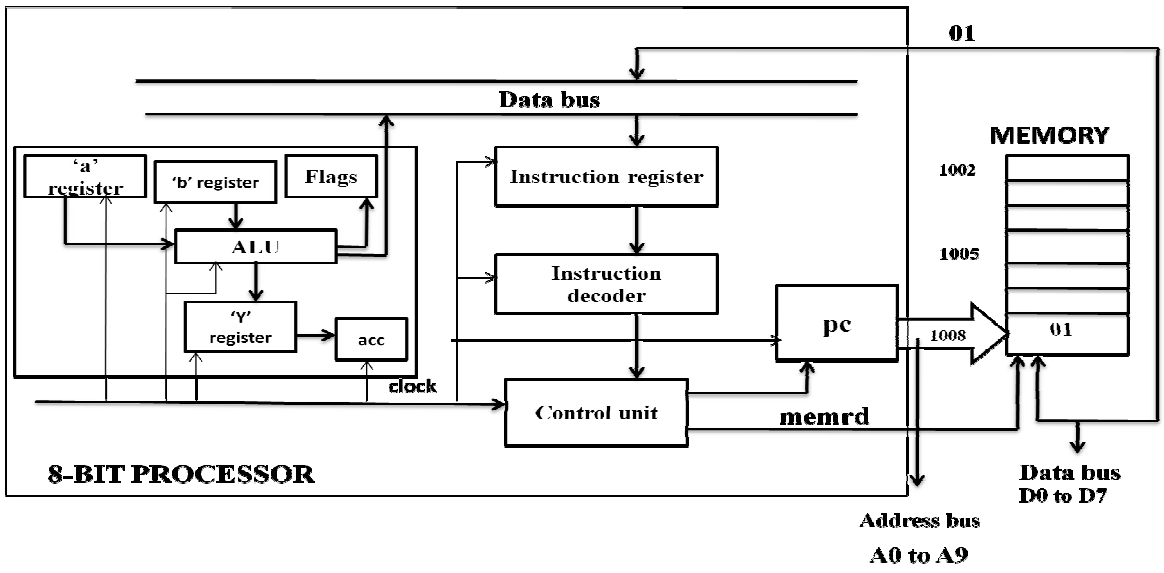

Figure.3 Block diagram of soft processor

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VI. SIMULATION RESULTS

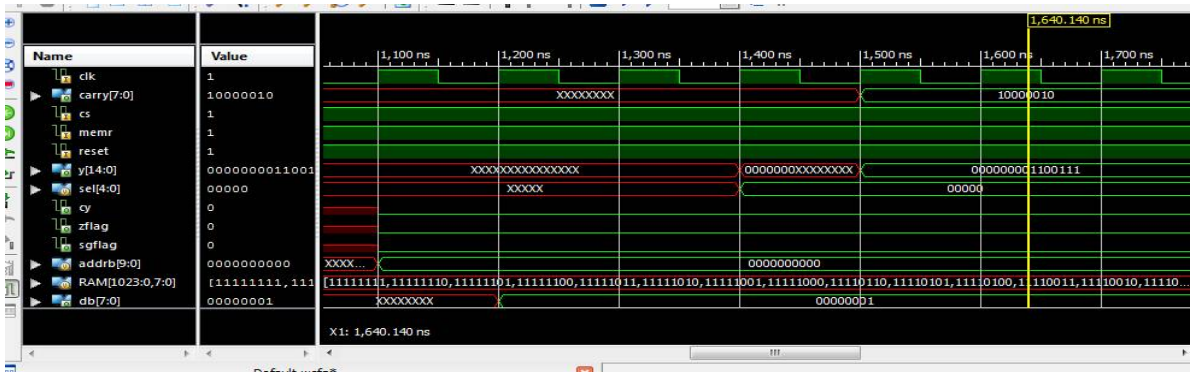

Figure. 4 Simulation result of soft processor (addition operation)

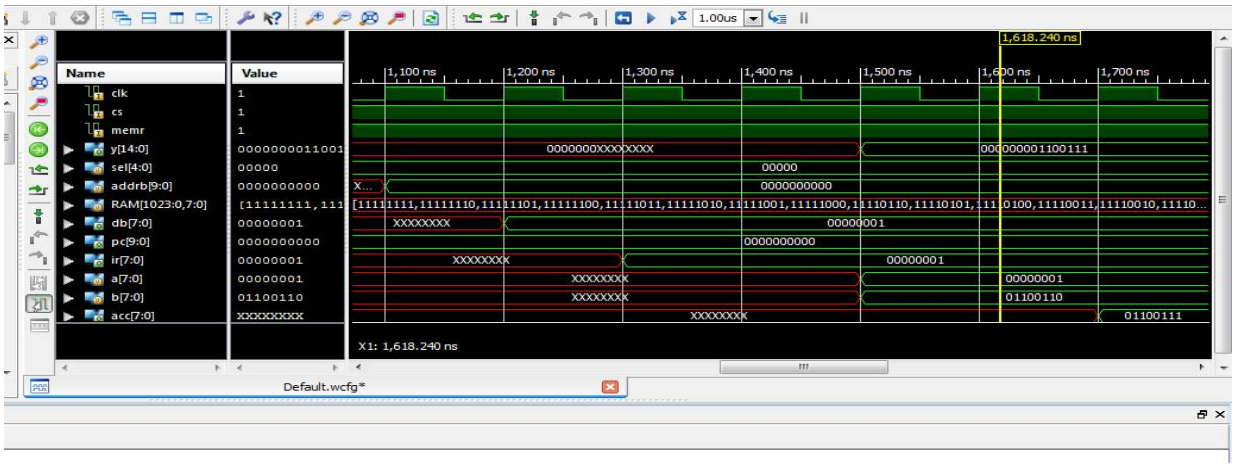

Figure.5 Simulation result of soft processor (addition operation)

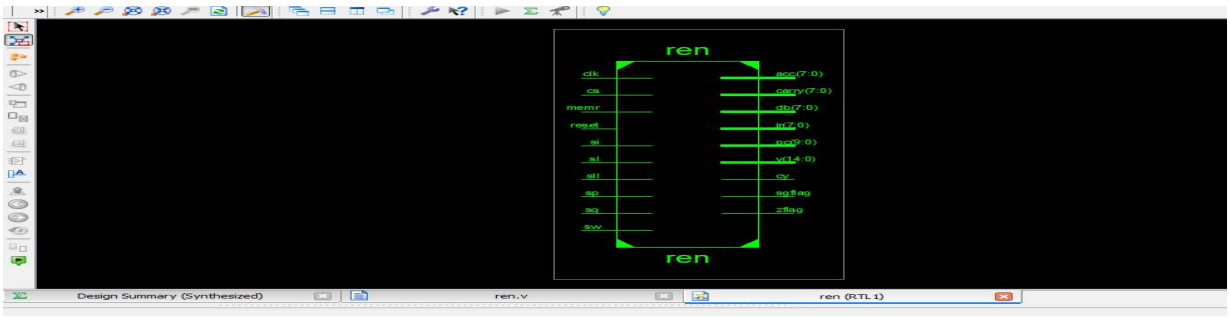

Figure.6 RTL of soft processor

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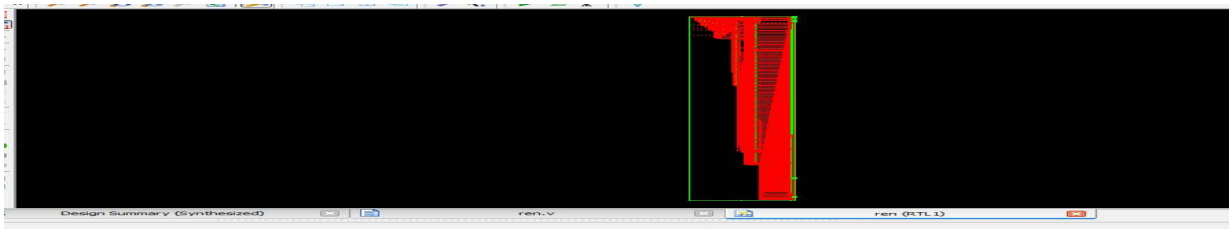

Figure.7 RTL of soft processor

VII. CONCLUSION

The 8-bit processor has been designed using verilog HDL and it is simulated using Xilinx ISE 12.2 software. All the components in the design were coded by using structural and behavioral modeling in verilog HDL language. It executes 22 different arithmetic and logical instructions such as addition, subtraction, increment, decrement, multiplication, square, ex-or, ex-nor, and, nand, nor, or, not, arithmetic shift left, arithmetic shift right, rotate left, rotate right, compare, logical shift left, logical shift right, add with carry, and subtract with carry. All the instructions in the design were coded using structural modeling in verilog HDL language. The processor which is designed operates at a frequency rate of 1MHz with a minimum period of 1000ns and totally 328 slices were utilizes.

VIII. FUTURE WORK

In future work, the floating point ALU can be added to the proposed processor thereby the 8-bit processor can be able to perform floating point operations. In addition to this further more instructions can be added, making the processor to perform all kinds of tasks.

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