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Folded Architecture for Adaptive Digital Filter

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ABSTRACT: Power consumption reduction is transpiring drift in area of VLSI digital signal processing. This gives rise to need of minimization of silicon area. Folding is an algorithm which reduces silicon chip area by combining various arithmetic operations into one operation by time scheduling technique. Least mean square algorithm alters coefficients of Adaptive filter in order to achieve desired output. Proposed work is focused on design of efficient VLSI architecture for LMS adaptive filter aims at reducing mainly area which results in power consumption reduction and hardware complexity. Adaptive LMS filter and Folded Adaptive LMS filter has been implemented in ISE and cadence tools. The design is evaluated in terms hardware resources, delay and power consumption. The numbers of adders and multipliers are reduced by 70%. Folded Adaptive filter with 90nm technology have been synthesized in cadence and the Simulation results shows that the designed filter achieves a 47.73% reduction in area, 24.01% reduction in power consumption, 50.44% reduction in Area-Delay product and 27.96% reduction in power-delay product, compared to the conventional filterwithout changing characteristics of filter.

KEYWORDS:VLSI, LMS, Adaptive filter, Area, Power, Delay, Cadence

I. INTRODUCTION

Today, every circuit has to face the power consumption issue, for both portable devices aiming at longer battery life and high-end circuits avoiding cooling packages and reliability issues that are too complex. As a result, for any chip design, power consumption has to be taken into account very seriously.

The performances and cost of any digital circuit depend on circuit design style. Therefore a careful choice of circuit design style is to be done for developing an architecture which has to establish optimal area-time-power trade-off. The increasing trend towards low power systems and high performance has forced researchers to come up with innovative design techniques which can achieve these objectives and meet the constricted system requirements.

An adaptive filter is a filter that self-adjusts its transfer function according to an optimizing algorithm. It adapts to changes in its input signals automatically according to a given algorithm. The algorithm will vary the coefficients according to a given criteria, typically an error signal to improve its performance. In essence an adaptive filter is a digital filter combined with an adaptive algorithm, which is used to modify the coefficients of the filter. Adaptive filters are used in many diverse applications in today's world for example telephone echo canceling, radar signal processing, and equalization of communication channels.

An adaptive filter is defined by four aspects: the signals being processed by the filter and the structure that defines how the output signal of the filter is computed from its input signal, the parameters within its structure that can be iteratively changed to alter the filter's input-output relationship and the adaptive algorithm that describes the way how parameters are adjusted from one time, instant to the next. The general adaptive filter system is shown in figure 1.

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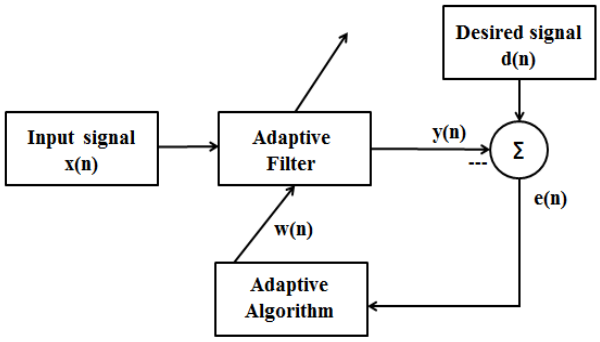

Fig. 1. General Adaptive filter systems

The remainder of this paper is organized as follows: The methodologies used are described in Section II. Proposed work in given in Section III. The Experimental results and discussion are done in Section IV. Finally, Section V represents the conclusion.

II. METHODOLOGY

Folding is a technique to reduce the silicon area by time multiplexing many algorithm operations into single functional units, such as adders and multipliers. The folding transformation provides a systematic technique to design control circuits for hardware in which several algorithm operations are time-multiplexed on a single functional unit.

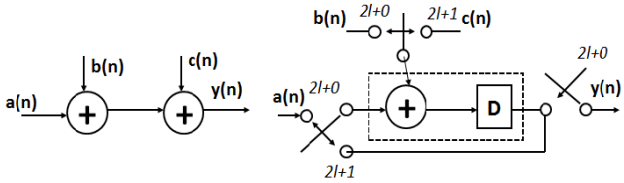

Fig. 2. (a) DSP program with two addition operations y(n) = a(n)+b(n)+c(n) and (b) Folded architecture in which two additions are folded into single hardware adder with one stage of pipelining.

Table I
Operation of the first six cycles of the folded hardware

Cycle	Adder Input (Left)	Adder Input (top)	System output
0	a(0)	b(0)	-
1	a(0)+b(0)	c(0)	-
2	a(1)	b(1)	a(0)+b(0)+c(0)
3	a(1)+b(1)	c(1)	-
4	a(2)	b(2)	a(1)+b(1)+c(1)
5	a(2)+b(2)	c(2)	-

The DSP program in figure 2(a) computes y(n) = a(n)+b(n)+c(n) . In figure 2(b) the addition operations shown in figure 2(a) are time multiplexed on a single pipelined order. One output sample is produced every 2 clock cycles, and one sample of each input signal is consumed every 2 clock cycles. As a result, an input sample must remain valid for 2

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clock cycles before changing. In general, the data on the input of the folded realization is assumed to be valid for N cycles before changing, where N is the number of algorithm operations executed on a single functional unit in hardware.

A. REVIEW OF LMS ADAPTIVE FILTER

Adaptive filtering techniques have been successfully used for many years. An adaptive filter is a self-designing and time-varying system that uses a recursive algorithm to continuously adjust its tap weights for operation in an unknown environment. It attempts to model the relationship between two signals in an iterative manner. Fig.1 shows a typical structure of the adaptive filter, which consists of two basic functional blocks: a digital filter to perform the desired filtering and an adaptive algorithm to adjust the tap weights of the filter.

The digital filter shown in Fig.1 can be designed using many different filter structures. To obtain simpler adaptive algorithms, finite impulse response (FIR) filters are preferable over infinite impulse response (IIR) filters.
The output signal of the digital filter is defined by the following equation:

$$\hat{y}(n) = X^T(n)\, W(n) \qquad (1)$$

Where, W(n)is the vector of the adaptive filter weights.

$$W(n) = [\, W_0(n)\ \ W_1(n) \ldots\ldots\ldots W_{L-1}(n)\,]^T \qquad (2)$$

The adaptive filter is updated using an adaptive algorithm, where the adaptation terms are added to the weight vector. The adaptation terms differ according the adaptive filter algorithms.

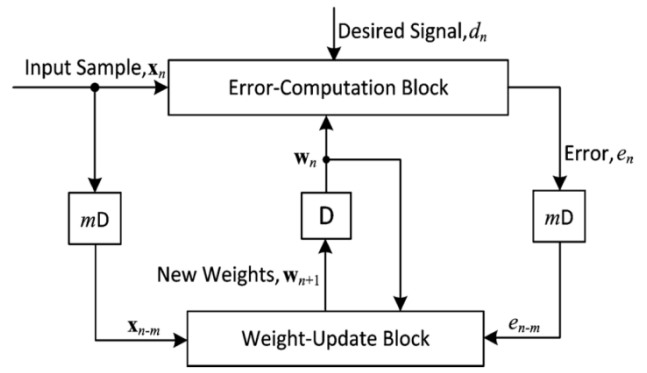

Fig. 3.Generalized block diagram of direct-form LMS adaptive filter

A generalized block diagram of direct-form DLMS adaptive filter is shown in Fig. 3. It consists of an error-computation block and a weight-update block .The number of delays "**m**" shown in Fig. 3 corresponds to the pipeline delays introduced due to pipelining of the error-computation block.

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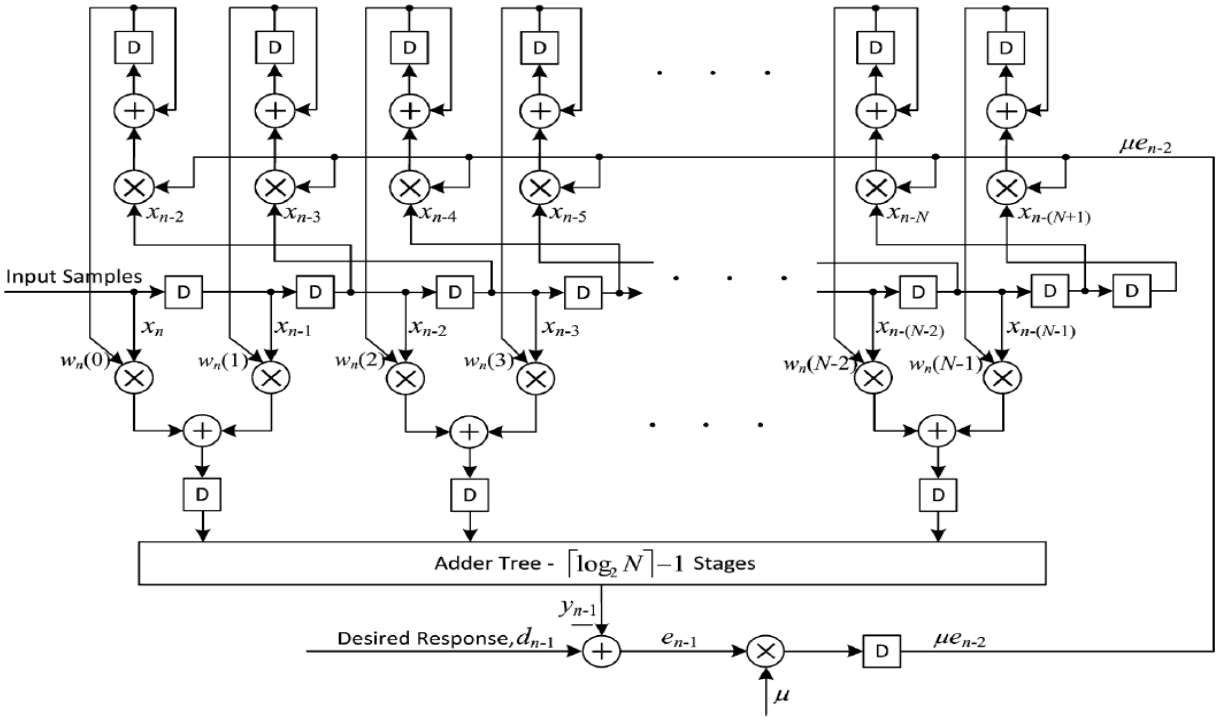

Fig. 4. Existing structure for direct-for LMS adaptive filter

The existing structure for a LMS adaptive filter is shown in Fig.4, which consists of three pipeline stages, where the first stage ends after the first level of the adder tree in the error-computation unit, and the rest of the error-computation block comprises the next pipeline stage. The weight-update block comprises the third pipeline stage. The two-adaptation-delay structure involves N/2 additional registers over the one-adaptation-delay structure. The critical path of this structure is the same as either that of the weight-updateC_{UPDATE} unit or the second pipeline stage, given by

$$T = \max \{T_{MULT} + \Delta, T_{AB}\} \qquad (3)$$

Where T_{AB}refers to the adder-tree delay of $\lceil \log_2 N \rceil - 1$ stages to add N/2 words along with the time required for subtraction in the error computation.

III. PROPOSED STRUCTURE

In this section, we discuss area- and power-efficient approaches for the implementation of direct-form LMS adaptive filters with folding technique. As shown in Fig. 3, there are two main computing blocks in the direct-form LMS adaptive filter, namely, i) the error-computation block and ii) the weight-update block. It can be observed that most of the area-intensive components are common in the error-computation and weight-update blocks: the multipliers, weight registers, and tapped-delay line.

The adder tree, subtractor and the adders for weight updating, which constitute only a small part of the circuit, are different in these two computing blocks. For the folded structure implementation, the computation of both these blocks is required to be performed in the same cycle. Moreover, since the structure is of the non-pipelined type, weight updating and error computation cannot occur concurrently.

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Therefore, the multiplications of both these phases could be multiplexed by the same set of multipliers,while the same registers could be used for both these phases if error computation is performed in the first half cycle, while weight update is performed in the second-half cycle.The time required for error computation is more than that of weight updating.

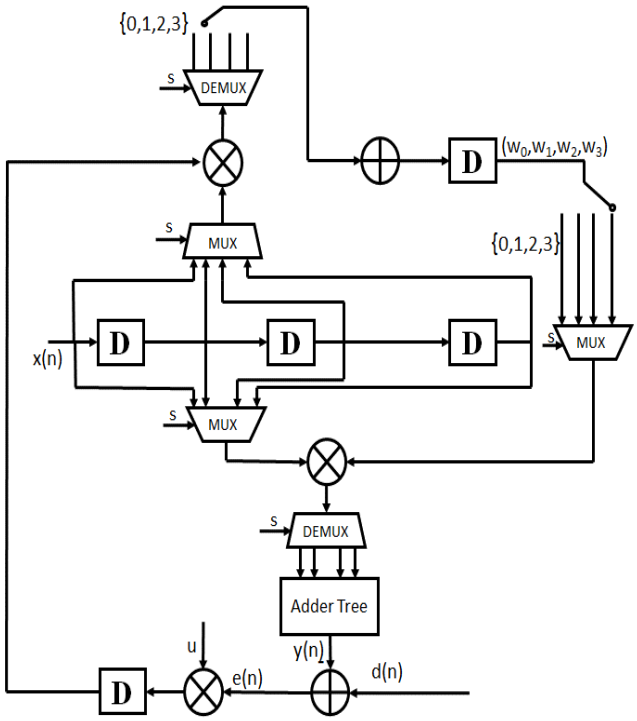

Fig. 5.Proposed structure of LMS Adaptive filter

The first half-cycle of each clock period ends with the computation of μe_n , and during the second half cycle, the μe_n value is fed to the multipliers though the multiplexors to calculate $\mu e_n x_n$ and de-multiplexed out to be added to the stored weight values to produce the new weights. The computation during the second half of a clock period is completed once a new set of weight values is computed.

The updated weight values are used in the first half-cycle of the next clock cycle for computation of the filter output and for subsequent error estimation. When the next cycle begins, the weight registers are also updated by the new weight values. Therefore, the weight registers are also clocked at the rising edge of each clock pulse.

The time required for error computation is more than that of weight updating. The system clock period could be less if we just perform these operations one after the other in every cycle. This is possible since all the register contents also change once at the beginning of a clock cycle, but we cannot exactly determine when the error computation is over and when weight updating is completed. Therefore, we need to perform the error computation during the first half-cycle and the weight updating during the second half-cycle.

The LMS algorithm, first proposed by Widrow and Hoff in 1960, is the most widely used adaptive filtering algorithm because of its simple structure, low computational complexity, good stability, and their performance can be defined by the cost function. The mean square error (MSE) has been the most extensively used criterion in the LMS algorithm and its variants. Using this cost function implicitly assumes that the error is a random variable with a Gaussian distribution.

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A linear adaptive filter consists of two basic processes. The first process involves performing convolution sum of the filter taps with the tap weights. The other process involves performing adaptation process on the tap weights.The weight update algorithm of an LMS algorithm is the most important block of LMS structure. The weight update equation is given by

$$\begin{pmatrix}\text{update value}\\ \text{of tap - weigth}\\ \text{vector}\end{pmatrix}=\begin{pmatrix}\text{old value}\\ \text{of tap - weight}\\ \text{vector}\end{pmatrix}+\begin{pmatrix}\text{learning -}\\ \text{rate}\\ \text{parameter}\end{pmatrix}\begin{pmatrix}tap-\\ input\\ vector\end{pmatrix}\begin{pmatrix}error\\ signal\end{pmatrix}$$

$$w(n+1)=w(n)+2\mu e(n)x(n) \qquad (4)$$

Before the filter coefficients can be updated the error must be calculated, simply find the difference between the desired response and the output of the adaptive filter. The error equation is given by

$$e(n)=d(n)-y(n) \qquad (5)$$

The minimum mean square error (MSE) is a metric indicating how well a system can adapt to a given solution. A small minimum MSE is an indication that the adaptive system has accurately modeled, predicted, adapted and/or converged to a solution for the system. The convergence rate determines the rate at which the filter converges to its resultant state. Usually a faster convergence rate is a desired characteristic of an adaptive system. Convergence rate is not, however, independent of all of the other performance characteristics. There will be a tradeoff, in other performance criteria, for an improved convergence rate. Stability is probably the most important performance measure for the adaptive system. Stability condition for LMS algorithm is given by,

$$0<\mu<\frac{2}{\text{input signal power}(\lambda_{\max})} \qquad (6)$$

where $\lambda_{\max}$ is the largest eigenvalue of the autocorrelation matrix of the input signal x(n).

IV. EXPERIMENTAL RESULTS AND DISCUSSION

Table II shows the comparison between the conventional and Folded LMS Adaptive filter in terms of the number of functional units i.e. adders & multipliers and the number of registers. As shown, the folding transformation results in a lower number of functional units compared to the conventional LMS Adaptive filter.

Table II
Comparison between the conventional and folded LMS Adaptive filter

Architecture	No. of functional units		Registers
	Adders	Multipliers	
Conventional	7	9	11
Proposed (Folded)	2	3	5

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It is seen that the number of adders are reduced by 71.42 % and multipliers by 66.66% and registers by 54.54%. This result definitely shows the reduction in silicon area as per objective and hence the power consumption is also reduced. The layout schematic of the proposed folded LMS adaptive filters is shown below,

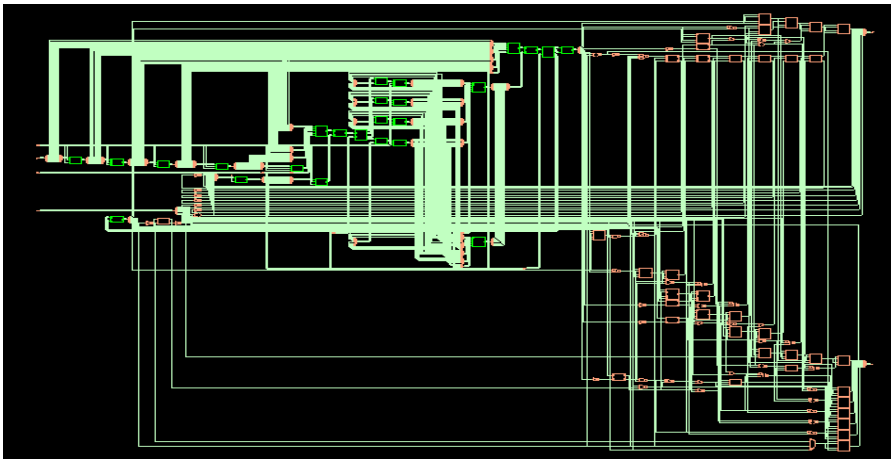

Fig. 6. Layout Schematic of Folded LMS Adaptive filter with 90nm technology

Table III

Core utilization of Layout schematic of Folded LMS Adaptive filter

No. of Cores	Single core
Total Cells utilized	712 cells
Area of single cell	26.5177669 μm^2
Total Area	18880.65 μm^2

The conventional and folded LMS adaptive filter is modeled in Verilog HDL and synthesized using ISE-Xilinx tool. Both the designs were synthesized using Cadence Encounter(R) RTL Compiler RC v13.10 and the results are shown in the table III.

Table IV

Synthesis result of conventional and proposed folded LMS Adaptive filter

Parameters	Conventional	Proposed
Area (μm^2)	36118.05	18880.65
Power (µW)	195.96067	148.90325
Delay (ns)	10.794	10.232
Area-Delay Product	389.85×10^3	193.18×10^3
Power-Delay Product	211.5×10	152.3×10

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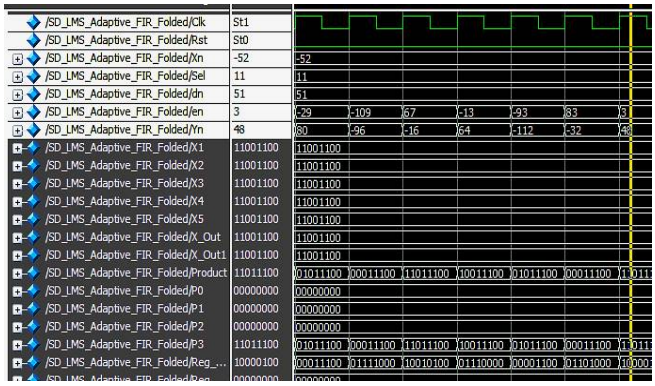

Fig. 7. Simulated output of proposed method in MODELSIM ALTERA 6.4a

The simulation result of the shown above is been implemented in MODELSIM ALTERA 6.4a. The input sequence to the architecture is x(n) and d(n). The multiplexer is controlled by the selection line.

1. Input sequence x(n) = 11001100 (-52)
2. Desired sequence d(n) = 00110011 (51)
3. Selection line Sel = 11 (3)
4. Output sequence y(n) = 00110000 (48)

The error equation is given by

$$e(n) = d(n) - y(n) \qquad (7)$$

Therefore, $e(n)$ =51-48=3

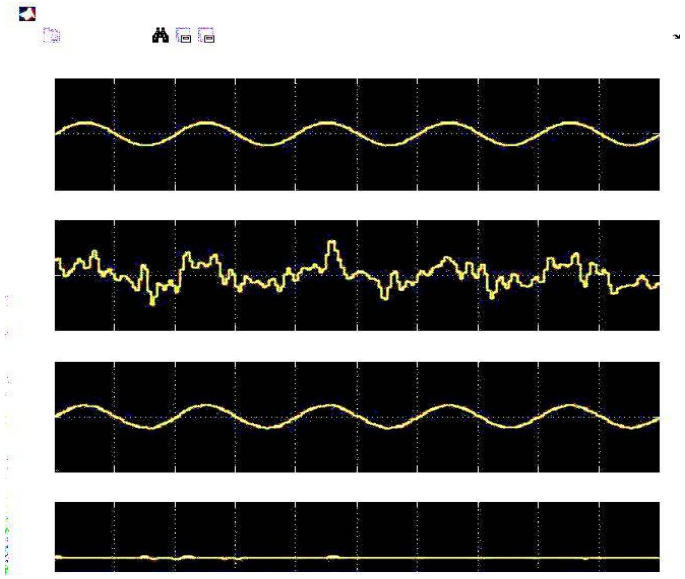

Fig. 8. Simulation output in MATLAB Simulink using System Generator

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V. CONCLUSION

In this work, a LMS adaptive filer was realized in a digital environment using Xilinx ISE tool. This implemented digital filter can be used in telecommunication for echo cancellation. Our results showS that the folded architecture of LMS adaptive filter significantly reduces the area of the filter, but there is a trade-off with the delay. Folded Adaptive filter with 90nm technology have been synthesized in cadence and the Simulation results shows that the designed filter achieves a 47.73% reduction in area, 24.01% reduction in power consumption, 50.44% reduction in Area-Delay product and 27.96% reduction in power-delay product, compared to the conventional filter without changing characteristics of filter.

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