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Design of Power Efficient Vedic Multiplier Based on RL: As Application of VLSI Technology

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ABSTRACT: Electricity is saved using reversible logic. Reversible logic produces distinct outputs for specified inputs without losing any information. No bits are lost, which lowers power use. In order to produce low-power products, reversible logic is used in this study's description of a revolutionary design for an 8-bit Vedic multiplier that operates quickly, efficiently, and with minimal power consumption. UT Sutra reduces latency, space, and power consumption by producing partial product and sum in a single step with fewer adders than a conventional booth and array multipliers. An 8-bit Vedic multiplier is produced by combining a 4-bit Vedic multiplier with modified ripple-carry adders. The recommended logic blocks simulate using Xilinx ISE and Verilog HDL.

KEYWORDS: Reversible Logic, Ripple carry Adder, Urdhva Tiryagbhyam Sutra, Vedic Mathematics.

I. INTRODUCTION

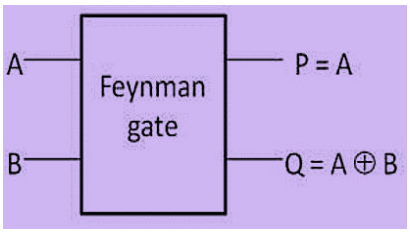
Reversible calculations use reversible gates and do not lose any information in the process. Using reversible logic results in a reduction in the amount of power used while also speeding up the response time of the system. Bennett demonstrated that reversible circuits eliminate the need for energy conservation measures inside a circuit. The use of reversible logic eliminates the loss of information as well as the waste of power. As reversible computing does not need the deletion of information, it does not lose any energy in the process.

Hence, reversible logic circuits avoid the loss of energy by recycling the energy that is produced by the system. In reversible circuits, fan-out and gate output-to-input feedback are not permitted in any configuration. Because of these constraints, it is possible to construct reversible circuits in the other direction. Both the input vector and the output vector are the same. The output vectors of an n-output reversible gate may be any one of 0 to 2n-1 different permutations.

Building computers using reversible logic presents an opportunity to eliminate the need for heat dissipation. Since it results in a loss of knowledge, reversible logic has a negative impact on teat formation. Calculations are able to be backtracked across time when using reversible logic. The reversible circuit contains n inputs and n outputs, and each pattern of input corresponds to a unique pattern of output. In reversible logic, garbage outputs (GO) are optimization and performance variables that do not contribute to the design. Quantum cast, often known as QC, refers to the cost of the circuit per primitive gate. The number of gates that may be reversed is indicated by the function's gate count or NG. Implementing logic functions requires a certain number of layers, which is referred to as the gate level.
Features and Design Constrain of Reversible Logic.

- Equal inputs and outputs characterize reversible logic.
- No fan-out. No feedback loops.
- Unused outputs are trash signals.
- Reduce the number of constants at gate inputs.

Basic reversible gates used in the design are listed below:



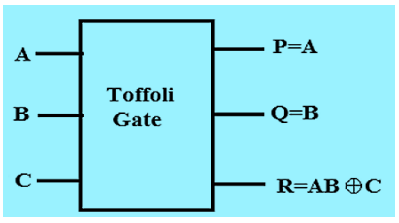
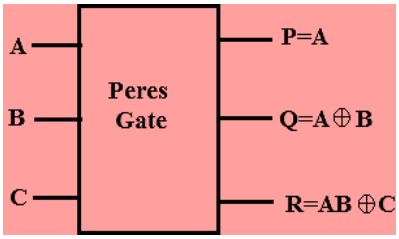


Fig.1:Feynman Gate (FG).

Fig.2:Toffoil Gate(TG).



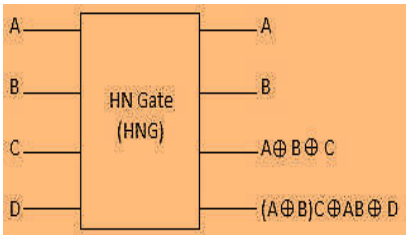


Fig.3:Press Gate (PG).

Fig.4: HN Gate (HNG).

II. LITERATURE REVIEW

For the literature survey point of view, some research articles are chosen for the study purpose. They as summarised as follows:

Landauer, R. (1961)[1] "argued that computing machines inevitably involve devices which perform logical functions that do not have a single-valued inverse. This logical irreversibility was associated with physical irreversibility and requires a minimal heat generation, per machine cycle, typically of the order of kT for each irreversible function. This dissipation served the purpose of standardizing signals and making them independent of their exact logical history. Two simple, but representative, models of bistable devices were subjected to a more detailed analysis of switching kinetics to yield the relationship between speed and energy dissipation, and to estimate the effects of errors induced by thermal fluctuations."

Bennett, C. H. (1973)[2] "shown that such machines may be made logically reversible at every step, while retaining their simplicity and their ability to do general computations. This result was of great physical interest because it makes plausible the existence of thermodynamically reversible computers which could perform useful computations at useful speed while dissipating considerably less than kT of energy per logical step. In the first stage of its computation the logically reversible automaton parallels the corresponding irreversible automaton, except that it saves all intermediate results, thereby avoiding the irreversible operation of erasure. The second stage consists of printing out the desired output. The third stage then reversibly disposes of all the undesired intermediate results by retracing the steps of the first stage in backward order thereby restoring the machine to its original condition. The final machine configuration thus contains the desired output and a reconstructed copy of the input, but no other undesired data.The foregoing results were demonstrated explicitly using a type of three-tape Turing machine. The biosynthesis of messenger RNA was discussed as a physical example of reversible computation."

Fredkin, E., & Toffoli, T. (1982). [3] "shows that it is ideally possible to build sequential circuits with zero internal power dissipation. After establishing a general framework, they discussed two specific models of computation. The first uses binary variables and was the conservative-logic counterpart of switching theory; this model proves that universal computing capabilities were compatible with the reversibility and conservation constraints. The second model, which was a refinement of the first, constitutes a substantial breakthrough in establishing a correspondence between computation and physics. In fact, this model was based on elastic collisions of identical "balls," and thus was formally identical with the atomic model that underlies the (classical) kinetic theory of perfect gases. Quite literally, the functional behaviour of a general-purpose digital computer can be reproduced by a perfect gas placed in a suitably shaped container and given appropriate initial conditions."

Shams, M., Haghparast, M., & Navi, K. (2008)[4]"proposed a novel 4x4 bit reversible Multiplier circuit. It wasfaster and has lower hardware complexity compared to the existing designs. In addition, the proposedreversible multiplier was better than the existing counterpart s in term of number of gates and number ofgarbage outputs. Haghparast and Navi recently proposed a 4x4 reversible gate called "MKG". Thereversible MKG gate can work singly as a reversible full adder. In current work,they use MKG gates toconstruct the reversible multiplier circuit. The proposed reversible multiplier circuit can multiply two 4-bitsbinary numbers. It can be generalized for NxN bit multiplication."

Babazadeh, S., & Haghparast, M. (2012)[5]"proposed a novel nanometric fault tolerant reversible binary coded decimal adder. To the best of our knowledge it was better than the only existing counterpart. The proposed circuit was

compared with the existing counterpart in terms of number of constant inputs and garbage outputs, delay and the quantum cost. All of the parameters were improved. All the circuits have nanometric scales."

Kunchigi, V., (2012)[6] "proposed a high-speed pipelined multiplier architecture. The pipelined architecture consists of 3 stages. 1ststage consists of the 4 - bit Vedic Multiplication unit. 2ndstage consists of partial products and carry. 3rd stage consists of adders and the result of the multiplication. This paper presented the efficiency of Urdhva Triyagbhyam Vedic method for multiplication which strikes a difference in the actual process of multiplication itself. It enables parallel generation of partial products and eliminates unwanted multiplication steps. The proposed algorithm was modeled using Verilog, a hardware description language. It was found that 11 logic cells are required to build nibble multiplier. The propagation time of the proposed architecture was found to be 4.585ns. Implementation has been done for the Xilinx FPGA device, Spartan-3E. The results show that multiplier implemented using Vedic multiplication is efficient in terms of area and speed compared to its implementation using Array and Booth multiplier architectures."

Lekshmi Viswanath, Ponni.M. (2012)[7] "proposed a reversible design of a 16-bit ALU. This ALU consists of eight operations, three arithmetic and five logical operations. The arithmetic operations include addition, subtraction, multiplication and the logical operations include NAND, AND, OR, NOT and XOR. All the modules were being designed using the basic reversible gates. The power and delay analysis of the various sub modules was performed and a comparison with the traditional circuits is also carried out."

Raju, B. R., & Satish, D. V. (2013)[8] "presented a high-speed complex 16 *16 multiplier design by using UrdhvaTiryakbhyam sutra. By using this sutra, the partial products and sums were generated in one step which reduces the design of architecture in processors. By using this sutra,they reduced the time with high extent when compare to array and booth multiplier. It can be implemented in many Digital Signal Processing (DSP) applications such as convolution, Fast Fourier Transform(FFT) filtering and in microprocessors. By using this method,they reduced the propagation delay in comparison with array-based architecture and parallel adder-based implementation which were most commonly used architectures.The main parameters were propagation delay and dynamic power consumption were calculated and found reduced."

Saligram, R., & Rakshith, T. R. (2013, April)[9] "proposed a multiplier design was always a challenging task; how many ever-novel designs were proposed, the user needs demand much more optimized ones. Vedic mathematics was world renowned for its algorithms that yield quicker results, be it for mental calculations or hardware design. Power dissipation was drastically reduced by the use of Reversible logic. The reversible Urdhva Tiryakbhayam Vedic multiplier was one such multiplier which was effective both in terms of speed and power. In this workthey aimed to enhance the performance of the previous design. The Total Reversible Logic Implementation Cost (TRLIC) was used as an aid to evaluate the proposed design. This multiplier can be efficiently adopted in designing Fast Fourier Transforms (FFTs) Filters and other applications of DSP like imaging, software defined radios, wireless communications."

Thapliyal, H., & Srinivas, M. B. (2005)[10] "Reversible logic is emerging as a promising area of research having its applications in quantum computing, nanotechnology, and optical computing. The classical set of gates such as AND, OR, and EXOR are not reversible. In this paper, a new 4 *4 reversible gate called "TSG" gate is proposed and is used to design efficient adder units. The proposed gate is used to design ripple carry adder, BCD adder and the carry look-ahead adder. The most significant aspect of the proposed gate is that it can work singly as a reversible full adder i.e. reversible full adder can now be implemented with a single gate only. It is demonstrated that the adder architectures using the proposed gate are much better and optimized, compared to their counterparts existing in literature, both in terms of number of reversible gates and the garbage outputs."

III.VEDIC MULTIPLIER

"The method of multiplication used in Vedic mathematics is more efficient than other approaches. The ideas of rapid and simple arithmetic are used in Vedic mathematics. It provides intricate algorithms for doing calculations. The UT sutra is implemented in the planned 8-bit multiplier (algorithms). UrdhvaTiryakbhayam literally translates to "vertically and crosswise." This UT sutra is acknowledged in the "Sthapatya- Veda," which is a supplement to the "Atharva Veda." This sutra does the multiplication of two decimal places. In order to convert the algorithm from analog to digital form, this sutra is used on the binary number. It's much simpler to use than the standard method of multiplication. The Urdhva Tiryakbhyam Multiplication Algorithms are generalized versions of multiplication formulae. "In both the

vertical and horizontal planes" Multiply the two ends of the line together, then add the carry from the line before it. All of the results from the various lines are combined together with the carrier that came before it. Although the other digits in the sum convey the information for the next step, the least significant digit in the total serves as one of the result digits. In the beginning, the carry bit is set to 0. Comparatively, the array and booth algorithms are more time-consuming. In order to function properly, the "NxN" multiplier requires "NxN" AND gates, "Nx(N-2)" full adders, and "N" half adders. Vedic multiplier requires (N-1) adders. The phases of the 4-Bit Vedic multiplier are shown in Fig.5.1]

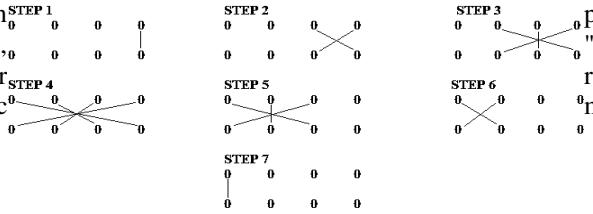


Fig.5: Vedic Multiplication Steps.

IV. PROPOSED ARCHITECTURE

"When multiplying two binary values, a reversible 8x8 Vedic multiplier that has been built would provide a 16-bit binary output. This output would be provided by the multiplier. In order to create the multiplier, a combination of Peres gates and Feynman gates was used in the development process. One of the most appealing features of UT design is the way it allows for the creation of unfinished products and the addition of features to take place at the same time.

The suggested block design for the 8x8 Vedic multiplier is shown in fig.6. Since it makes use of three 8-bit ripples carry adders and four 4x4 Vedic multipliers, it is easy to put into practice. In contrast to multipliers of the array and booth kinds, the construction of the recommended 8x8 multiplier is quite simple and makes effective use of the available resources. Every single multiplier incorporates reversible PG and TG gates within its design in order to facilitate its building. Moreover, RCA is built with HNG gates being used in its construction. Consequently, it doesn't matter which way you go about applying the patterns. 720 is the amount that this item costs in quantum terms.

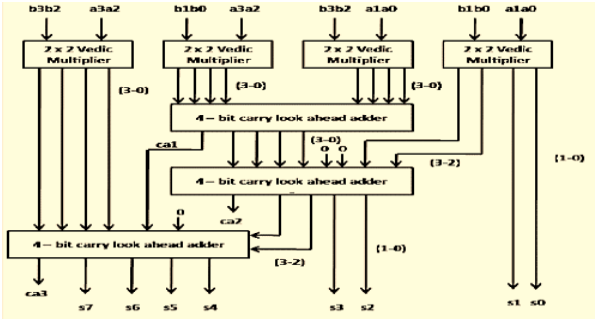


Fig.6.Proposed Block Diagram for the 8x8 Vedic Multiplier.

An HNG gate is going to be included into the design of the reversible adder that is going to be built. In the HNG gate, if the fourth input, D, is given a value of zero as a constant and inputs are given through A and B and carried to the third input C, then it acts as a reversible one-bit full adder, and output is taken from R and S respectively. This occurs when the fourth input is given a constant value of zero and inputs are given through A and B and carried to the third input C. If the inputs are delivered via A and B and transported to the third input C, then this outcome will take place.
A ripple carry adder, also known as an HNG gate with two 8-bit inputs and a carrier that is propagated from the list of a significant bit (LSB) to the most significant bit (MSB), are used to produce the proposed 8-bit reversible adder. The

LSB is the least significant bit and the MSB is the most significant bit. The most significant bit, or MSB, is the bit that comes after the most important one. The reversible ripple-carry adder has a very small footprint, and its construction is

rather basic; as a result, ripple-carry adders are often employed for reasons related to cascading. Since each HNG gate is capable of acting as a full adder for just one bit, you will need a total of eight HNG gates in order to build an 8-bit ripple carry adder. This is because each HNG gate serves the role of a complete adder. The output is indicated by the letters S0-S7, and the letter "g" may be found in the garbage to indicate it. The 4-bit ripple carry adder is constructed using the HNG gate in addition to its other components. The suggested adder produces a total of sixteen values that are considered to be garbage, and doing so results in a quantum cost of forty-eight. The reversible 8-bit ripple carry adder that was mentioned before may be seen shown in Fig.7.

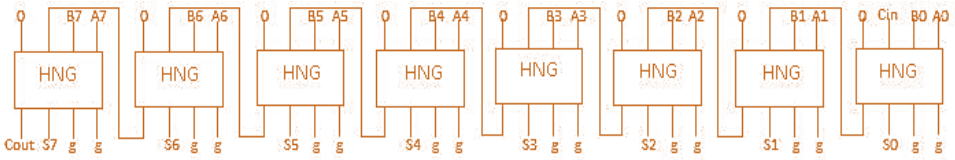


Fig.7: Proposed 8-Bit RCA using HNG Gate.

V. DESIGN AND IMPLEMENTATION

The VHDL programming language is used to draught the design architectures that are then implemented with the help of the Xilinx ISE 14.5 tool. The ISIM tool that is bundled with Xilinx is used to do simulations of the VHDL codes, and the results of these simulations are then transferred to the Spartan LX45 board so that they may be processed. The RTL designs of an 8x8 Vedic multiplier and an 8-bit ripple carry adder are seen in Fig.8 and 9, respectively.

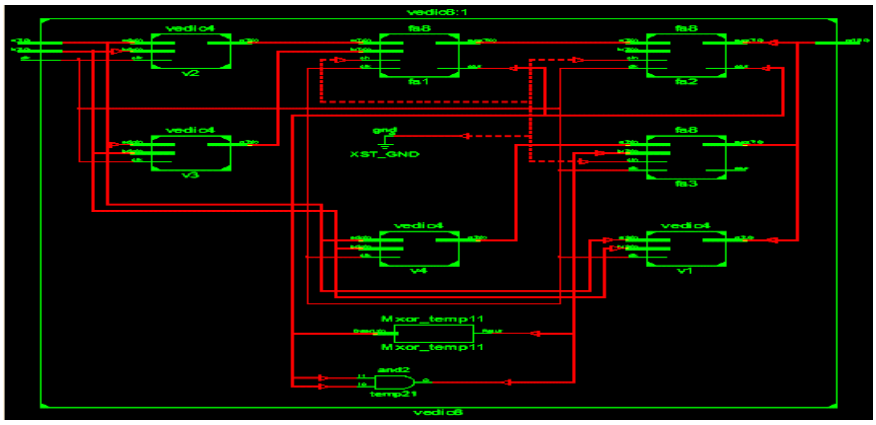


Fig.8:RTLof Proposed 8x8 VedicMultiplier.

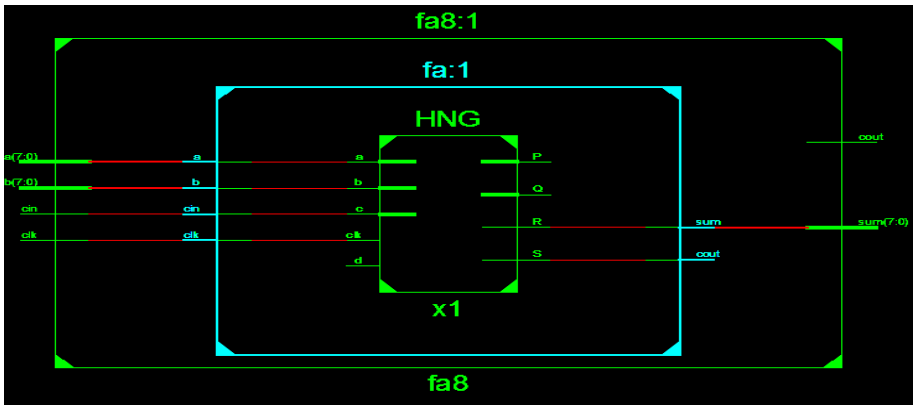


Fig.9: RTLofProposed8-bitRCA.

The RTL description of a circuit, which stands for "Resister Transfer Level," provides information on the registers of the circuit as well as the order in which transfers occur between the registers. The RTL description, on the other hand, does not provide any information on the hardware that is used to carry out these operations. It plays a role in determining not only the size of the registers but also the total number of registers that are put into use." [11]

VI. RESULTS AND DISCUSSION

"Verilog HDL is used to model each and every one of the blocks. Xilinx ISE ISim is used in order to validate the simulation results obtained from the suggested design. This accomplishes functional verification of the conceptual design, which allows the developer to synthesise their ideas and carry out timing analysis.

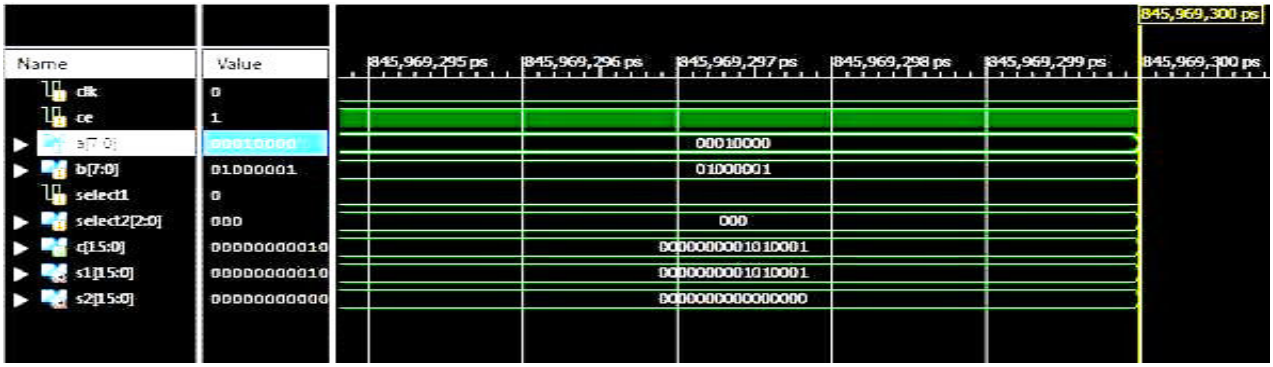


Fig.10. Simulation result of 8-bit RCA

.

Observations were made on the time delay and power consumption of suggested 8-bit reversible, nonreversible, and adders. The results of these observations were compared in Table 1.

Table 1. Time and Power Comparisons of the Proposed Logic

Parameters	Irreversible RCA	Ref.[7]	Proposed ReversibleRCA
Time Delay (ns)	11.2 ns	7.88 ns	7.2 ns
Power (mw)	0.047	0.0114	0.0101

According to the findings that were presented earlier, the reversible ripple carries adder that was presented is more time- and power-efficient than the design that was proposed in [7], as well as irreversible logic. This conclusion was reached as a result of the findings that were presented earlier.

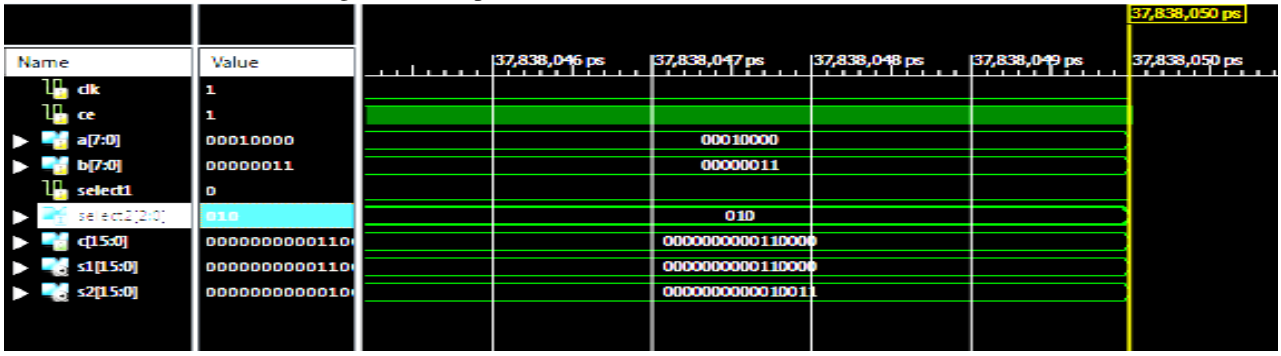


Fig.11: Simulation Result of 8x8 Vedic Multiplier.

Table 2 presents a comparison of the 8-bit reversible Vedic multiplier with the conventional multiplier (Booth), as well as the reversible multiplier [7], in terms of aspects such as time delay, power consumption, and space utilization.

Table 2. Comparison of Multiplier Designs.

Parameters	Conv.Booth Multiplier	Ref [7]	Proposed Multiplier
Time Delay	27.72ns	21.44ns	20.249ns
Power (mw)	0.430mw	0.299mw	0.278mw
Area (No.slice LUTs.)	171	--	108

The standard 8-bit booth multiplier and architecture given in [7] are outperformed by the suggested 8-bit reversible multiplier, which is superior in terms of both efficiency and optimization.
As a comparison to the standard booth multiplier, the power dissipation, speed, and space utilization in terms of LUT have each been improved by 36.36 percent, 27.93 percent, and 35.6 percent, respectively. In addition, compared to the design, the new concept offers an increase of 6.2% in power and 6% in speed [7]. The 3*3 reversible gates, which are the essential blocks of the proposed architecture, are responsible for the reduction in power dissipation. However, Viswanath and Ponni used a 4*4 gate in their previous work [7], therefore this is not the case (TSG).
Both the proposed Low Power Reversible Vedic multiplier and the conventional booth structure are realized through the use of the programming language VHDL, simulated and synthesized through the use of Xilinx ISE 14.5, and ultimately realized through the utilization of a Spartan xc6slx45-2csg324 FPGA kit."[7]

VI. CONCLUSION

The design that has been recommended has lower power consumption as well as increased operational speed when compared to the alternative design. This is due to the use of fast reversible logic-based adders, which consume less power and take up less space, as well as Vedic multipliers, which have lower levels of complexity in their underlying hardware. When it comes to the Vedic multiplier, having a smaller total number of adders results in less wasted space and power, in addition to the fact that the computation process is sped up. The proposed logic is implemented in the form of a program that is written in Verilog HDL. This program is then simulated and synthesized with the assistance of the software known as Xilinx ISE 14.5i. It was established, as a consequence of the output that was generated, that the suggested approach required roughly 36 percent less power, had an area that was 37 percent smaller, and performed approximately 26 percent better than the traditional circuit. In addition to that, the approach that was suggested consumed 5 percent less power while increasing speed by 7 percent.

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