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A Novel Method for Area Efficient N-Bit Full Comparator Using Quantum-Dot Cellular Automata

S.Shyline Mabel Gnanalilly, K.Vijayananth,

M.E, Dept. of Applied Electronics, V.V College of Engineering, Tisaiyanvilai, Tamilnadu, India

Assistant Professor, Dept. of ECE, V.V College of Engineering, Tisaiyanvilai, Tamilnadu, India

ABSTRACT: Quantum-dot Cellular Automata (QCA) an innovative technology that allows placement of logic circuits using semi conductive quantum dots. The attractive features such as smaller size, reduced area and high speed computation makes QCA suitable for implementing various arithmetic circuits. Several design methods have been proposed to implement electronic circuits by considering the trade-offs between overall area and speed. This paper focus on a novel method for implementation of n-bit full binary comparator using QCA. The novelty proposed in this paper involves formulation of new basic logic equation required for comparison of two n-bit inputs. The proposed system in this paper exhibits low power consumption, reduced delay and overall area.

KEYWORDS*:* Binary comparator, Quantum-dot Cellular Automata, Arithmetic circuits.

I.INTRODUCTION

Now-a-days Technology has made the world a global village. We can access anyone in seconds from thousands of miles. This is all because of the development of technology in modern era, where everything seems advanced. We can see how specializes our life is after the development and innovation of technology. QCA is one such technology that serves as an alternative to conventional CMOS technology. A new efficient architecture for the design of fast low-cost single-clock-cycle binary comparators[4] was designed and this novel architecture is 12% faster and requires 69% less transistors, but this architecture is not suitable for computing n-bits. The novelty proposed in this paper focuses on n-bit comparison of inputs which is implemented by QCA logic using majority gates and inverters.

II. BACKGROUND AND RELATED WORKS

The basic element of a nanostructure based on QCA is a square cell with four quantum dots and two free electrons. The latter can tunnel through the dots within the cell, but, owing to Coulombic repulsion, they will always reside in opposite corners [1], thus leading to only two possible stable states, also named polarizations. Locations of the electrons in the cell are associated with the binary states 1 and 0. Adjacent cells interact through electrostatic forces and tend to align their polarizations. However, QCA cells do not have intrinsic data flow directionality. Therefore, to achieve controllable data directions, the cells within a QCA design are partitioned into the so-called clock zones that are progressively associated with four clock signals, each phase shifted by 90◦. This clock scheme, named the zone clocking scheme, makes theQCA designs intrinsically pipelined, since each clock zone behaves like a D-latch [20].QCA cells are used for both logic structures and interconnections that can exploit either the coplanar cross or the bridge technique [1], [2], [6], [31], [32]. The fundamental logic gates inherently available within the QCA technology are the inverter and the majority gate (MG). Given three inputs *a*, *b* and *c*, the MG performs the logic function reported in (1) provided that all input cells are associated with the same clock signal *clkx* (with *x* ranging from 0 to 3), whereas the remaining cells of the MG are associated with the clock signal *clkx*+1 $M(a, b, c) = a \cdot b + a \cdot c + b \cdot c$ (1) There are several QCA designs of comparators in the literature [22]–[28]. A 1-bit binary comparator receives two bits *a* and *b* as inputs and establishes whether they are equal, less than or greater than each other. These possible states are represented through three output signals, here named *A*eq*B*, *A*big*B*,*B*big*A*, that are asserted, respectively, when $a = b$, $a>b$, and$a<b$.

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Full comparators are those that can separately identify all the above cases, whereas non-full comparators recognize just one or two of them. As an example, the comparator designed in [22] and depicted in Fig. 1(a) can verify only whether $a = b$. Conversely, the circuits shown in Fig. 1(b) and (c), proposed in [23] and [24], are full comparators. The latter also exploits two 1-bit registers D to process n-bit operands serially from the least significant bit to the most significant one. With the main objective of reducing the number of wire crossings, which is still a big challenge of QCA designs [33]–[35], in [25] the universal logic gate (ULG) $f(y1, y2, y3) = M(M(y1, y2 , 0),M(y1, y3 , 1), 1)$ was proposed and then used to implement the comparator illustrated in Fig. 1(d). It is worth noting that, two n-bit numbers $A(n-1:0) = an-1 \ldots a0$ and $B(n-1:0) = bn-1 \ldots b0$ can be processed by cascading n instances of the 1-bit comparator. Each instance receives as inputs the ith bits ai and bi (with $i = n - 1, \ldots, 0$) of the operands and the signals Abig$B(i-1:0)$ and Bbig$A(i-1:0)$. The former is asserted when the subword $A(i-1:0) = ai-1 \ldots a0$ represents a binary number greater than $B(i-1:0) = bi-1 \ldots b0$. In a similar way, Bbig$A(i-1:0)$ is set to 1 when $A(i-1:0) < B(i-1:0)$. The outputs Abig$B(i:0)$ and Bbig$A(i:0)$ directly feed the next stage. It can be seen that this circuit does not identify the case in which $A = B$, therefore it cannot be classified as a full-comparator. The design described in [26] exploits a tree-based (TB) architecture and exhibits a delay that in theory logarithmically increases with n. The 2-bit version of such designed comparator is illustrated in Fig. 1(e). Also the full comparator proposed in [27] exploits a TB architecture to achieve high speed. As shown in Fig. 1(f), where 4-bit operands are assumed, one instance of the 1-bit comparator presented in [23] is used for each bit position. The intermediate results obtained in this way are then further processed through a proper number of cascaded 2-input OR and AND gates implemented by means of MGs having one input permanently set to 1 and 0, respectively. Analyzing existing QCA implementations of binary comparators it can be observed that they were designed directly mapping Fig. 1. QCA-based comparators presented in: (a) [22]; (b) [23]; (c) [24]; (d) [25]; (e) [26]; (f) [27]. the basic Boolean functions consolidated for the CMOS logic designs to MGs and inverters, or ULGs. Unfortunately, in this way the computational capability offered by each MG could be underutilized [13], [36], [37]. As a consequence, both the complexity and the overall delay of the resulting QCA designs could be increased in vain.

III. MODULES OF n-BIT FULL COMPARATOR

A common and very useful combinational logic circuit is that of the Digital Comparator circuit. Digital or Binary Comparators are made up from standard AND, NOR and NOT gates that compare the digital signals present at their input terminals and produce an output depending upon the condition of those inputs.

A 1-bit binary comparator receives two bits a and b as inputs and establishes whether they are equal, less than or greater than each other. These possible states are represented through three output signals, here named AeqB, Abig ,BbigA, that are asserted, respectively, when $a = b$, $a>b$ and $a<b$. Full comparators are those that can separately identify all the above cases, whereas non-full comparators recognize just one or two of them.

The first proposed comparator exploits a cascade-based (CB) architecture. To explain better how the overall computation is performed, the schematic diagram illustrated in Fig. 3 is provided.It shows a possible implementation of a 32-bit comparator based on the proposed theory. The n-bit CB full comparator designed as proposed here uses: $n/3$ instances of T1 and/or T2; $n/3$ cascaded instances of T4 through which the signals Abig$B(n-1:0)$ and Bbig$A(n-1:0)$ are computed; and one instance of C2, needed to compute also Aeq$B(n-1:0)$. Circles visible in Fig. 3 indicate the additional clock phases that have to be inserted on wires to guarantee the correct synchronization of the overall design. As it is well known, the number of cascaded MGs within the worst computational path of a QCA design directly affects the delay achieved. In fact, each MG introduces one clock phase in the overall delay. From Fig. 2, it can be seen that the modules T1 and T2 contribute to the computational path with one inverter and two MGs. Each instance of T4 introduces one more MG, whereas C2 is responsible for one MG and one inverter. As a consequence, the critical computational path of the novel n-bit CB full comparator consists of $n/3+ 3$ MGs and 2 inverters. As an example, the 32-bit implementation depicted in Fig. 3 has the worst-case path made up of 13 MGs and 2 inverters. As always happens in CB computational architectures, the number of MGs within the computational path of the above described comparator linearly increases with n.

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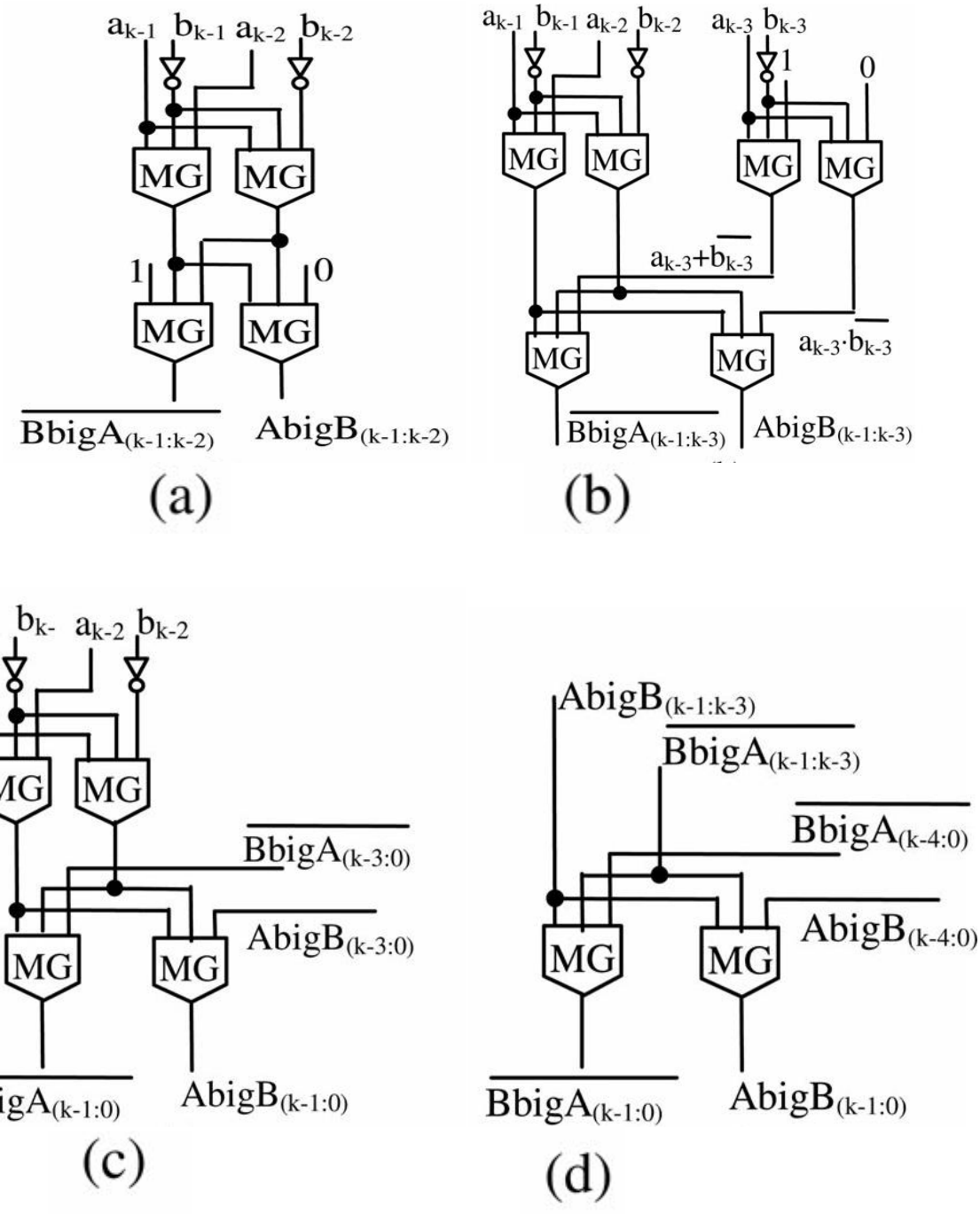

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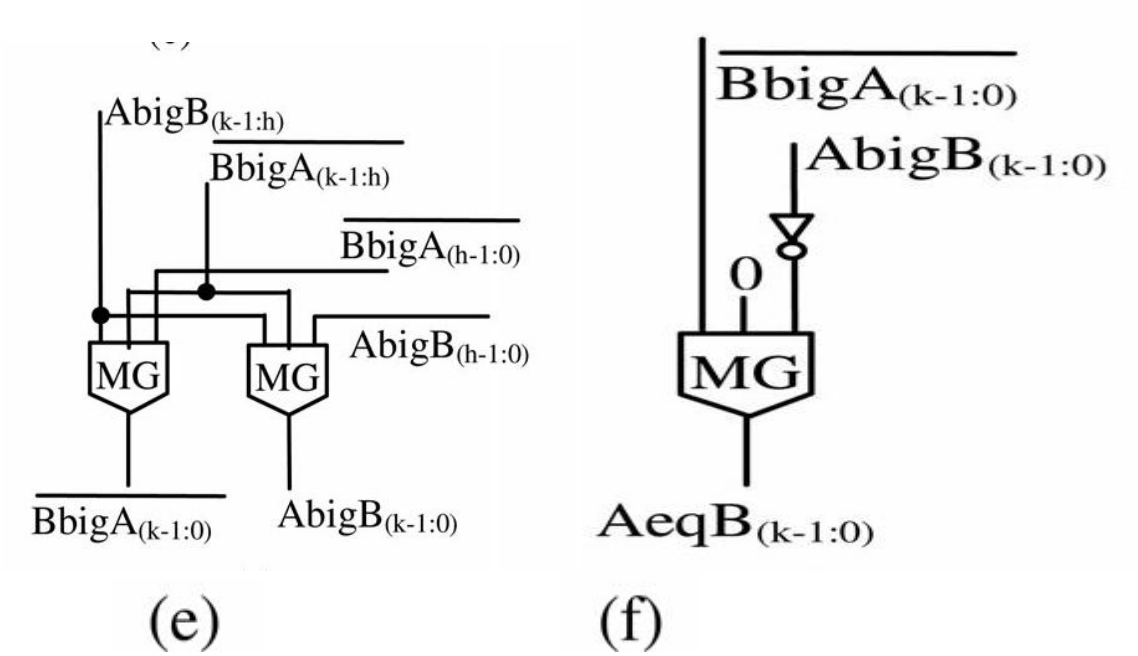

Fig. 1. QCA modules: (a) T1; (b) T2; (c) T3; (d) T4; (e) C1; and (f) C2.

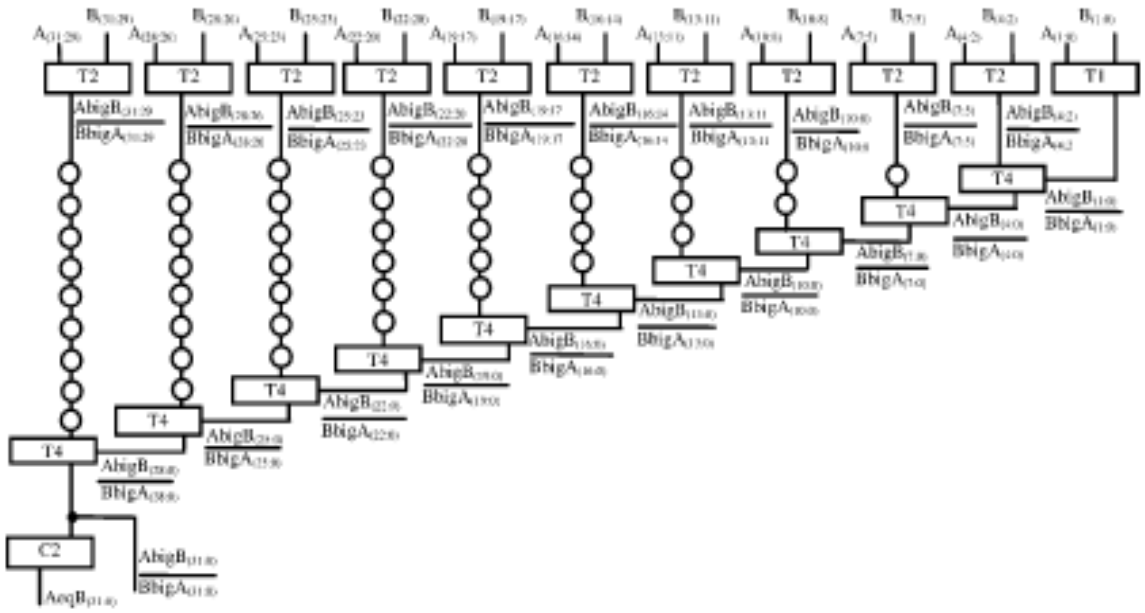

Fig. 2. Novel 32-bit full comparator.

IV. RESULTS AND DISCUSSIONS

Preliminary results obtained for the novel comparators at several operands word lengths are reported in Table I. It can be seen that, exploiting the formulations introduced in this paper, the novel comparators can achieve lower complexity than their competitors, especially when wider operands are processed in order to achieve robust QCA designs, a maximum of 15 or 16 cascaded cells per clock zone should be used. As a consequence, overlong wires introduce

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additional clock phases that, depending on the operands word length, can significantly exceed the number of cascaded MGs reported in Table I, thus compromising the actually achievable speed performances. As shown in the following, the novel comparators have been implemented in QCA taking this aspect into account. Proper layout strategies have been adopted that allow the number of additional clock phases due to overlong wires to be limited to 1 independently of the operands word length and in cascade-based architecture.

TABLE:I COMPARATION RESULTS

Design	Computational capability	n	Complexity		MGs in the worst computational path
			MGs	Inverters	
Others	A≥B	2	4	2	2
		4	11	4	3
		8	26	8	4
		16	57	16	5
		32	120	32	6
	Full	2	10	7	4
		4	22	13	5
		8	46	25	9
New CB	Full	2	5	3	3
		4	11	5	4
		8	21	9	5
		16	43	17	8
		32	85	33	13

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